Vidyavardhini's College of Engineering & Technology, Vasai

Department of Electronics & Telecommunication Engineering

TE/V SEM 2024-2025

Course name/Code: Digital VLSI Lab/ECL503

Name of Student: Chinmayi Umesh Upadhya **Roll No.** 48

List of Experiments

Sr. No.	Name of Experiment	DOP	DOC	Marks	Sign
	Basic Experiments				
1	To plot drain and transfer characteristics of a MOSFET using LTspice software.	16/7	30/07	19	
2	To plot and observe drain and transfer characteristics of MOSFET based on Threshold voltage, Process Trans conductance parameter.	23/7	30/07	18	
3	To plot drain characteristics of MOSFET and observe Channel length modulation effect.	30/7	6/08	18	
4	To plot and observe drain current of MOSFET for different types of scaling.	6/08	13/08	19	
5	To plot transfer and transient characteristics of resistive load inverter.	13/08	20/8	18	
	To plot voltage transfer and transient characteristics of CMOS inverter.	20/08	03/09	18	
	To realize NAND and NOR gates and verify truth table in LTspice software.	03/9	17/9	18	
	Realize any expression using any logic style and verify its operation using LT spice.	03/9	17/9	18	
	To realize 2:1 mux using Pass transistor logic in LT spice software.	17/9	24/9	18	
	To implement D-Latch using CMOS logic and verify truth table in LT spice software.	24/9	01/10	18	
	To Sketch Layout of CMOS Inverter using Microwind.	24/9	01/10	18	
	To sketch layout of NMOS and PMOS pass transistor switch, transmission gate using	01/10	8/10	18	

	Microwind.				
13	To Sketch Layout of NAND and NOR gates using Microwind.	01/10	8/10	18	
14	Realize and draw layout any expression using any logic style, using Microwind.	01/10	8/10	18	
15	To implement half adder using LT Spice and draw layout, verify the truth table.	8/10	17/10	18	

List of Assignments

1	Assignment 01	7/8	23/8	9	
2	Assignment 02	23/8	23/8	10	
3	Assignment 03	11/10	17/10	10	

List of Quiz and Activity

1	Quiz 01- Self learning	12/9	12/9	7/9	
2	Quiz 02	12/9	12/9	13/15	
3	Quiz 03	3/10	3/10	8/10	
4	Quiz 04	3/10	3/10	10/10	
5	Quiz 05	23/10	23/10	8/10	
6	Quiz 06	23/10	23/10	9/10	
7	Crossword Puzzle on Datapath Component	23/10	23/10	10/10	

23/10/2

Course In-charge

Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmayi Umesh Upadhya
Roll No. :	48
Practical No.:	01
Title of Practical:	To plot drain & transfer characteristics
Date of Submission:	16/7/24
Date of Correction:	30/7/24

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	05
Journal work and timely submission	10	09
Total	20	19

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

Checked by

Name of Faculty: Ms. Shaistha Khanam

Signature:

Date: 30/07/24

Rollno:- 48

Vidyavardhini's College of Engineering & Technology

Department of Electronics & Telecommunication Engineering

Experiment No.1

Aim: To plot drain and transfer characteristics of a MOSFET using LTspice software.

Software: LTspice software.

Theory: The MOSFET is the most common semiconductor device in digital and analog circuits, and the most common power device. MOSFET scaling and miniaturization has been driving the rapid exponential growth of electronic semiconductor technology and enables high-density integrated circuits (ICs) such as memory chips and microprocessor. The transfer characteristic curve can locate the gate voltage at which the transistor passes current and leaves the OFF state.

MOSFET operates by creating or "enhancing" its conductive channel between the source and drain regions producing a type of MOSFET commonly called an n-channel Enhancement-mode MOSFET, which simply means that unless we bias them positively on the gate (negatively for the p-channel), no channel current.

Figure 1(a) and (b) show the transfer characteristics (drain-to-source current I_{DS} versus gate-to-source voltage V_{GS}) of n-channel Enhancement-type MOSFETs. From this, it is evident that the current through the device will be zero until the V_{GS} exceeds the value of threshold voltage V_T. This is because under this state, the device will be void of channel which will be connecting the drain and the source terminals. Under this condition, even an increase in V_{DS} will result in no current flow as indicated by the corresponding output characteristics (I_{DS} versus V_{DS}) shown by Figure 1b. As a result, this state represents nothing but the cut-off region of MOSFET's operation.

Next, once V_{GS} crosses V_T, the current through the device increases with an increase in I_{DS} initially (Ohmic region) and then saturates to a value as determined by the V_{GS} (saturation region of operation) i.e., as V_{GS} increases, even the saturation current flowing through the device also increases. This is evident by Figure 1b where I_{DSS2} is greater than I_{DSS1} as $V_{GS2} > V_{GS1}$, I_{DSS3} is greater than I_{DSS2} as $V_{GS3} > V_{GS2}$, so on and so forth. Further, Figure 1b also shows the locus of pinch-off voltage (black discontinuous curve), from which V_P is seen to increase with an in-
in V_{GS}.

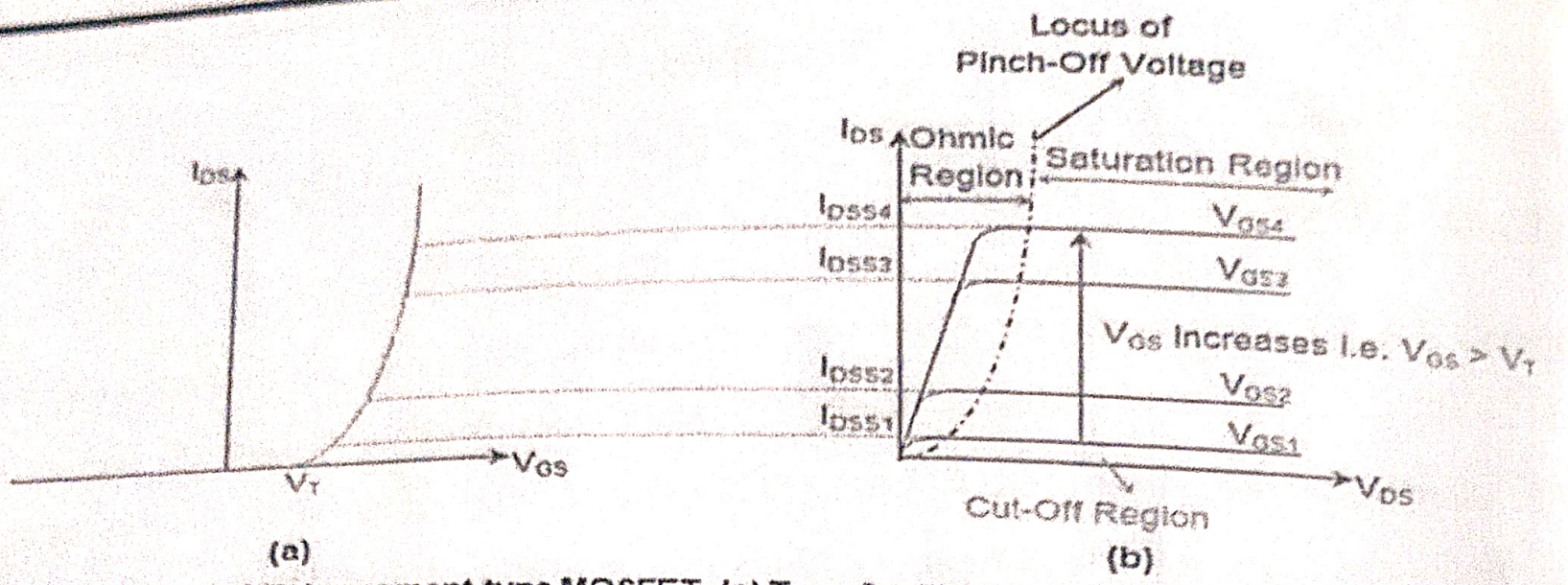
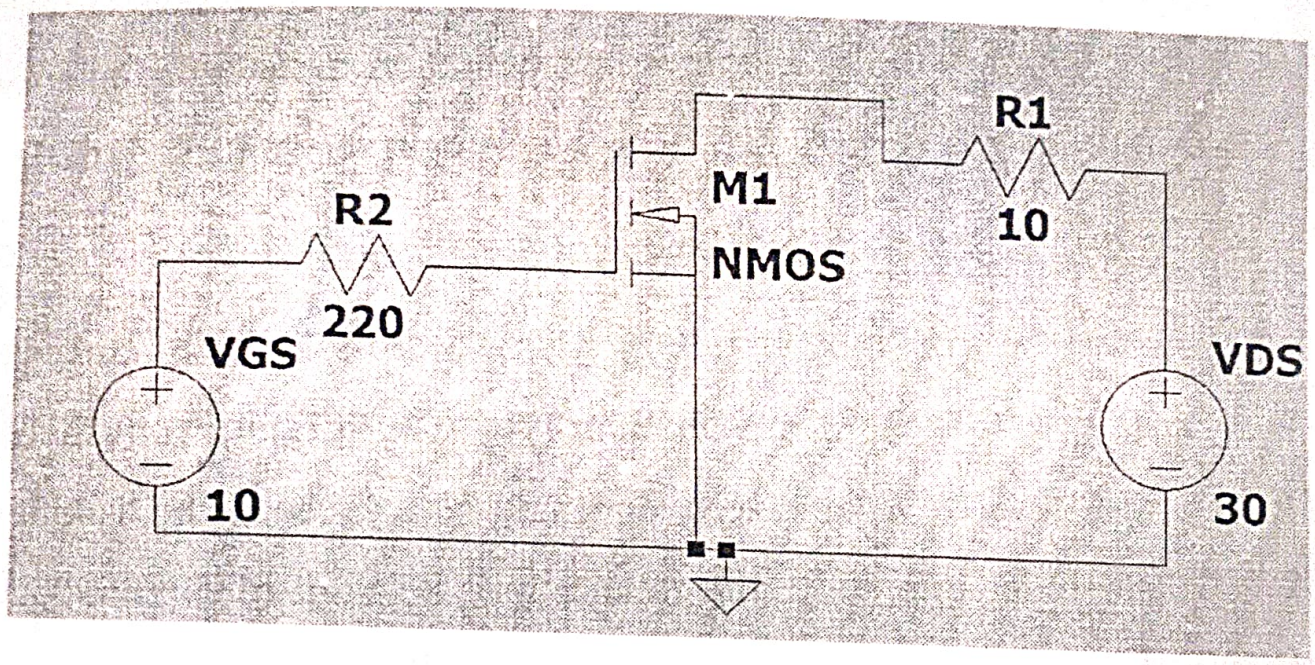


Figure 1 *n*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

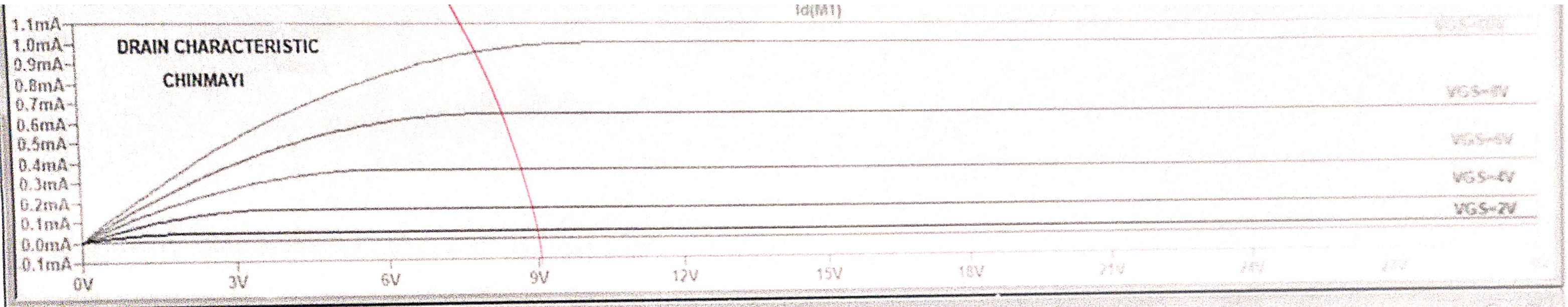
Circuit Diagram:



LTspice:LTspice is a high-performance SPICE simulation software, schematic capture and waveform viewer with enhancements and models for easing the simulation of analog circuits. Included in the download of LTspice are macro models for most Analog Devices switching regulators, amplifiers, as well as a library of devices for general circuit simulation.

Procedure: -

1. Make new schematic.
2. Place component as per circuit diagram and connect it.
3. Select component values.
4. Select simulation profile as DC sweep.
5. Transfer characteristics vary VGS voltage from 0 – 10V in the step of 1Volt and plot the characteristics.
6. Drain characteristics Vary VDS 0-30v in the step of 0.1V and VGS from 0 – 10V in the step of 2V. Plot drain characteristics.



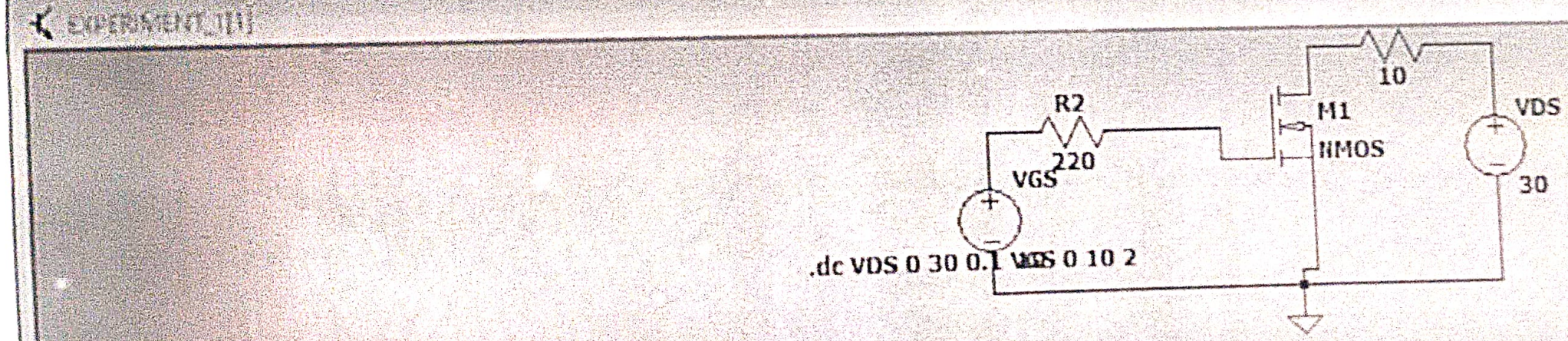
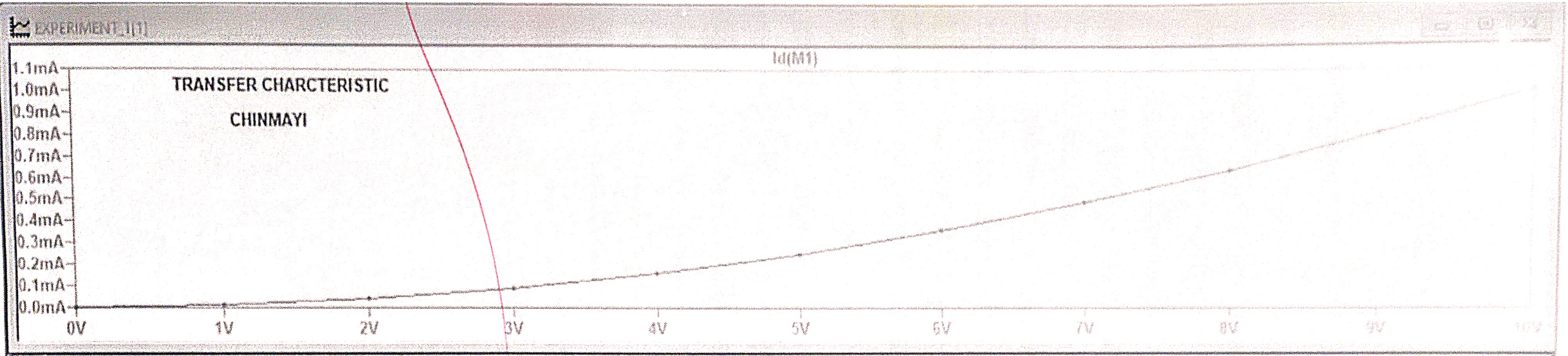


Figure 2.Drain Characteristics



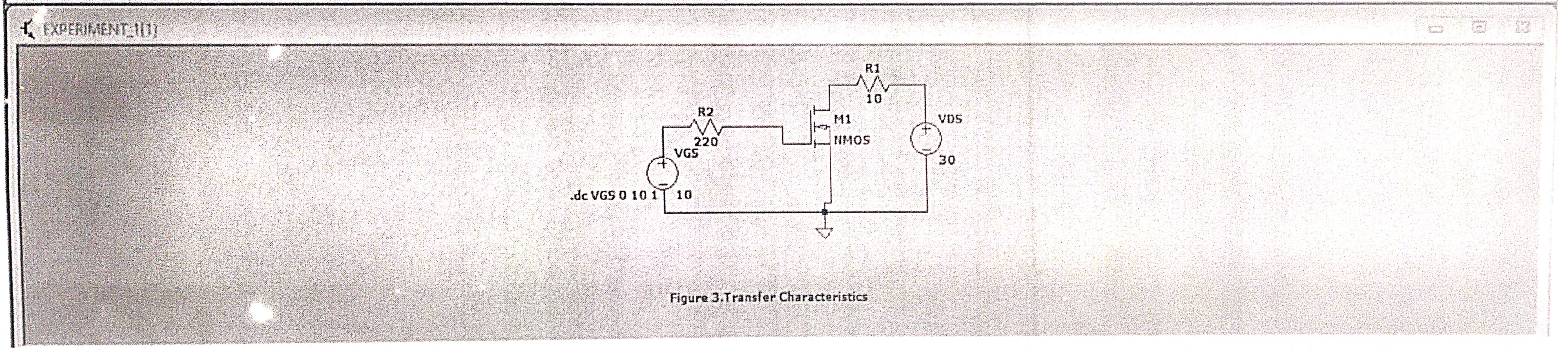


Figure 3.Transfer Characteristics

Result analysis and Conclusion:-

In this experiment, the drain & transfer characteristic of N MOSFET. In drain characteristic of N MOSFET, after $V_{GS} > V_T$ the channel is formed and In current increases rapidly with increase in V_{GS} & V_{DS} but after some time due to deplection layer the I_D current remains constant with increase of V_{DS}. With the graph we understand the drain characteristic with the region formed and In transfer character the graph is exponentialy increasing after $V_{GS} > V_T$ when channel is formed as electron is released increases.

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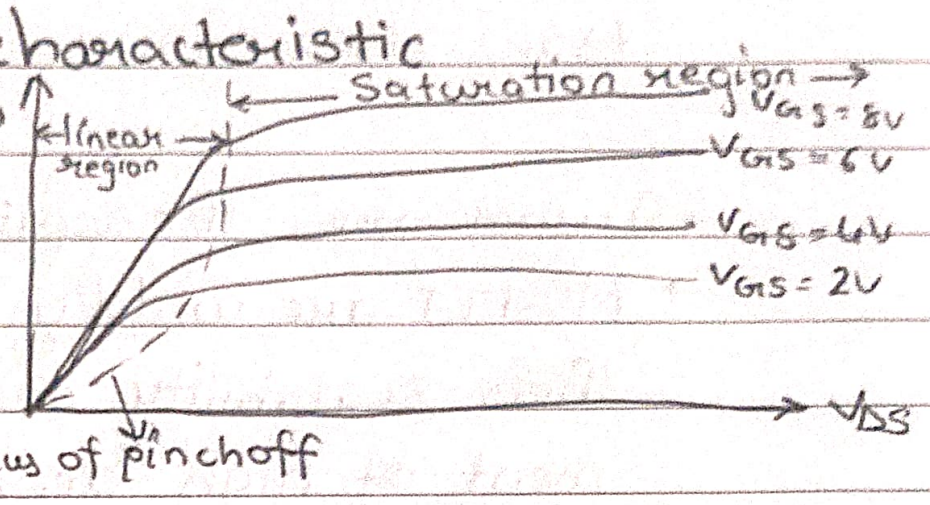
POST Experiment questions:-

Q1) Explain different region of Drain characteristic

→ There are two region formed in Drain characteristic due to locus of pinchoff. 1 linear region - In linear region, the I_D current increases with increase in V_{DS} as well as V_{GS}. The I_D current grows exponteinal till locus of pinchoff. In linear region, it is used as a amp^r which increases the amp^r of the signal. 2. Saturation region - In saturation region, the I_D current increases sightly with increase of V_{GS} but remains constant with increase in V_{DS}. I_D remains constant so it is known as saturation region. So, for switch application is done in saturation region.



I_D formula for linear = $\frac{\mu_n C_{ox}}{2} \times \frac{W}{L} (2(V_{GS} - V_T) V_{DS} - V_{DS}^2)$

I_D formula for saturation region = $\frac{\mu_n C_{ox}}{2} \times \frac{W}{L} (2(V_{GS} - V_T)^2$

There is another region which is cutoff region. Cutoff region- when V_{GS} is below the threshold voltage V_T, no channel formed and the drain current I_D is zero.

Q2) Why MOSFET is called as field effect transistor?

→ MOSFET are called field effect transistor because they use an electric field to control the flow of current. The gate voltage generates an electric field that modulate the conductivity of a semiconductor channel between the source & drain terminals. By altering the electric field, the gate voltage effectively opens or close

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the channel allowing or blocking current flow. This fu
modulation mechanism distinguishes MOSFET's from ot
transistors which relay on current flow for contro

Q3) what are the applications of MOSFET.

→ MOSFET are widely used in digital and analog circuit d
their scalability and efficiency. They are integral to the
-ment of high-density integrated circuit (IC) like me
chips and microprocessors. MOSFET's are used in powe
electronics for switching and amplifying signals, maki
crucial in power supplies, motor controllers & RF a
Their ability to efficiently switch & amplify signals underlies
diverse applications.

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Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DWLST

Name of Student:	Chinmayi Umesh Upadhya
Roll No. :	48
Practical No.:	02
Title of Practical:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	04
Understanding	5	05
Journal work and timely submission	10	09
Total	20	18

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

Checked by

Name of Faculty: Ms. Shaista khanam

Signature: S. Khanam

Date: 30/07/24

Experiment No. 2

Aim: To plot and observe drain and transfer characteristics of MOSFET based on Threshold voltage, Process Trans conductance and Channel length modulation parameter.

Software: - LTspice software.

Theory:

Transfer Characteristics:

It is plot of gate to source voltage (V_{GS}) and drain current (I_D) as shown in figure1.The current I_D is zero for VGS less then V_{GS} (th) i: e threshold voltage. When the V_{GS} is made positive, the drain current I_D increases slowly at first, and then much more rapidly with an increase in V_{GS}.

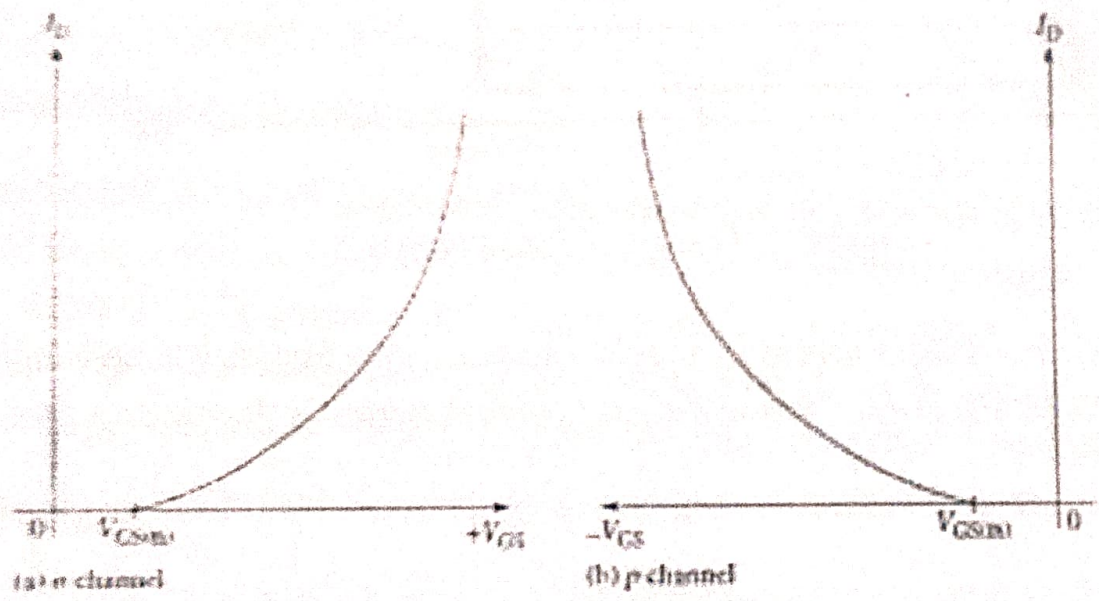


Figure 1. Transfer Characteristics

Drain Characteristics:

The drain characteristics of a MOSFET are drawn between the drain current I_D and the drain source voltage V_{DS}. The characteristic curve is as shown in figure 2 for different values of input voltage Vgs. Characteristics is divided into two regions, ohmic region and saturation region.

The lowest curve is When V_{GS} is lesser than $V_{GS\ (TH)}$, I_D is approximately zero. This region is called cut off as device is off. When V_{GS} is greater than V_{GST}, the device turns- on and the drain current I_D is controlled by the gate voltage. The characteristic curves have almost vertical and almost horizontal parts. The almost vertical components of the curves correspond to the ohmic region (linear region), and the horizontal components correspond to the constant current region.

Thus E-MOSFET can be operated in either of these regions *i.e.*, it can be used as a variable-voltage resistor (WR) or as a constant current source. In saturation region drain current is constant for increased value of drain to source voltage. Very high value of drain to source voltage and drain current can lead to breakdown of region causing excessive current which damage the MOSFET.

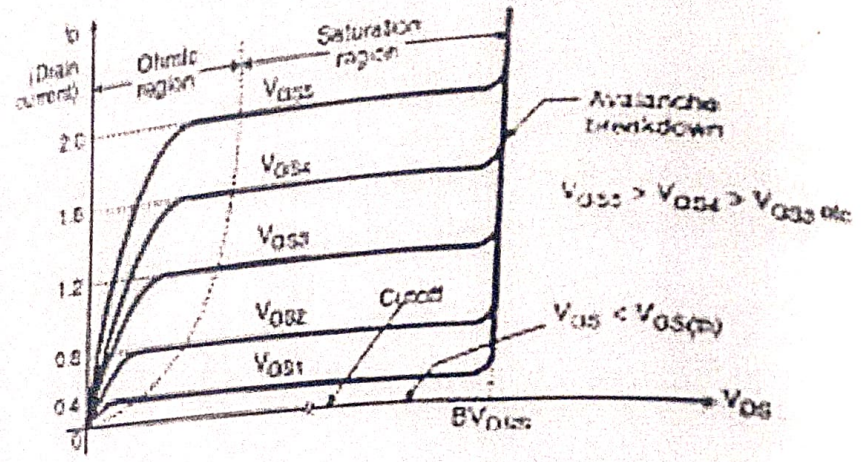


Figure 2. Transfer Characteristics

When V_{DS} is increased, the drain current I_D should increase, but due to the applied V_{GS}, the current is controlled at certain level. Hence the gate current controls the output drain current.

Current equation for linear and saturation region for N- channel MOSFET is given by following equation 1 and 2.

$$I_D(Linear) = \frac{1}{2}\mu nCox\frac{W}{L}((2(V_{GS}-V_T)V_{DS}-V_{DS}^2) \quad (1)$$

$$I_D(Saturation) = \frac{1}{2}\mu nCox\frac{W}{L}(V_{GS}-V_T)^2 \quad (2)$$

Threshold voltage:

Threshold voltage is the voltage needed on the Gate terminal of the enhancement type MOSFET to form a thin channel beneath the gate electrode (between Source & Drain terminals), so that current can flow between both the terminals. Threshold voltage is the voltage needed to turn

the device. As the MOSFET is voltage controlled current source, the output current will depend on the gate voltage applied.

Process trans conductance:

Process Trans conductance parameter is the product of mobility of electrons in channel (μn) and oxide capacitance (cox). (Measured in υ/S). It is given by equation 3.

$$Kn = \mu nCox \quad (3)$$

Where Cox = εox / tox

εox is permittivity of oxide and tox is thickness of oxide layer.

As tox is increased or decreased oxide capacitance changes hence changing process transconductance.

Channel-length modulation parameter:

Channel-length modulation (λ) is important because it decides the MOSFET output resistance. The resistance of the channel is inversely proportional to its width-to-length ratio; reducing the length leads to decreased resistance and hence higher current flow. Thus, channel-length modulation means that the saturation-region drain current will increase slightly as the drain-to-source voltage increases. Drain current for channel length modulation is given by equation 4.

$$I_D = \frac{1}{2}\mu nCox\frac{W}{L}(V_{GS}-V_T)2(1+\lambda V_{DS}) \quad (4)$$

Procedure: -

1. Make new schematic.
2. Place component as per circuit diagram and connect it.
3. Select component values.
4. Select simulation profile as DC sweep.
5. Transfer characteristics vary VGS voltage from 0 – 10V in the step of 1Volt and plot the characteristics.
6. Drain characteristics Vary VDS 0-30v in the step of 0.1V and VGS from 0 – 10V in the step of 2V. Plot drain characteristics.
7. Vary the value of Threshold voltage, Process Trans conductance and Channel length modulation parameter and observe its effect on transfer characteristics and drain characteristics.

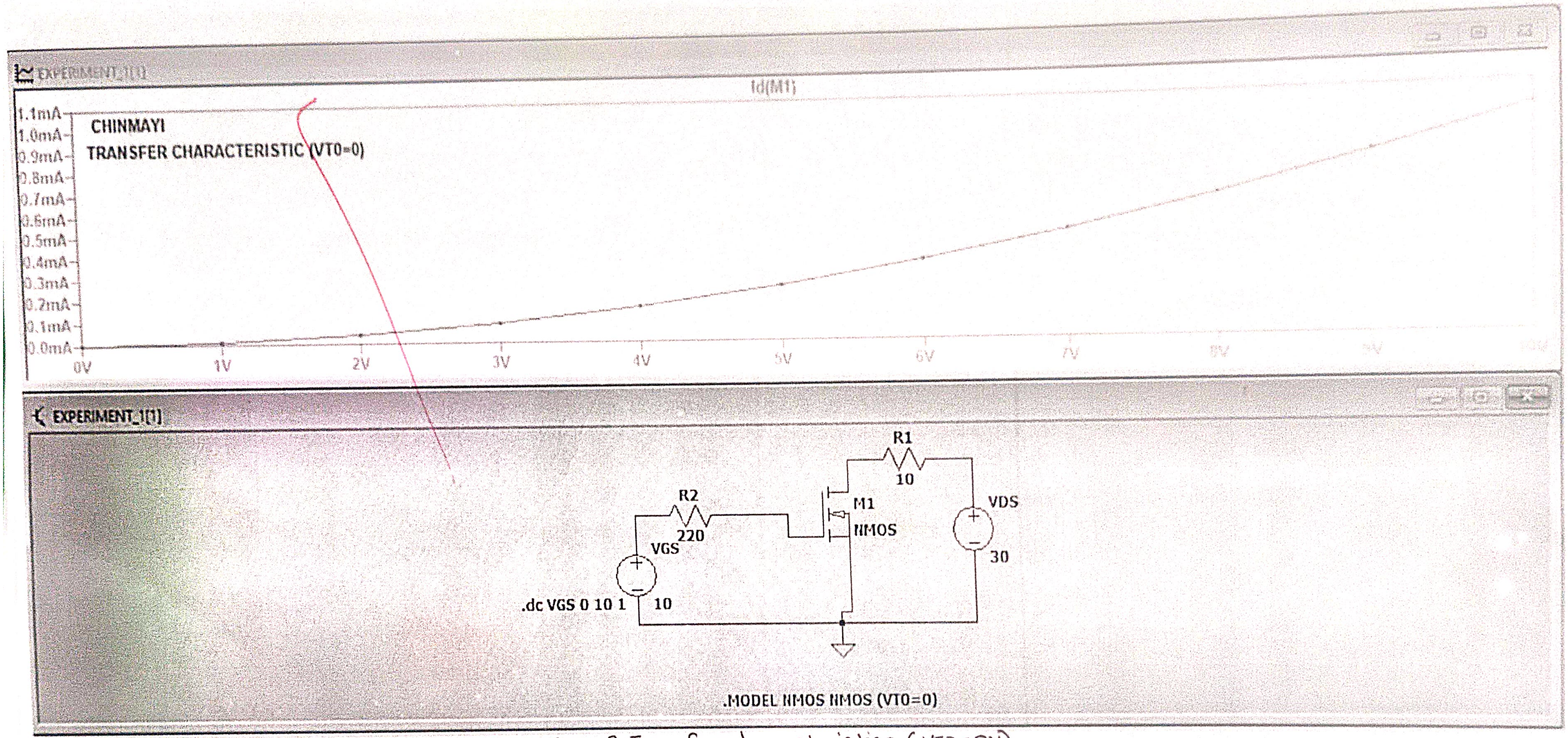


Figure 3. Transfer characteristics (VTO = 0V)

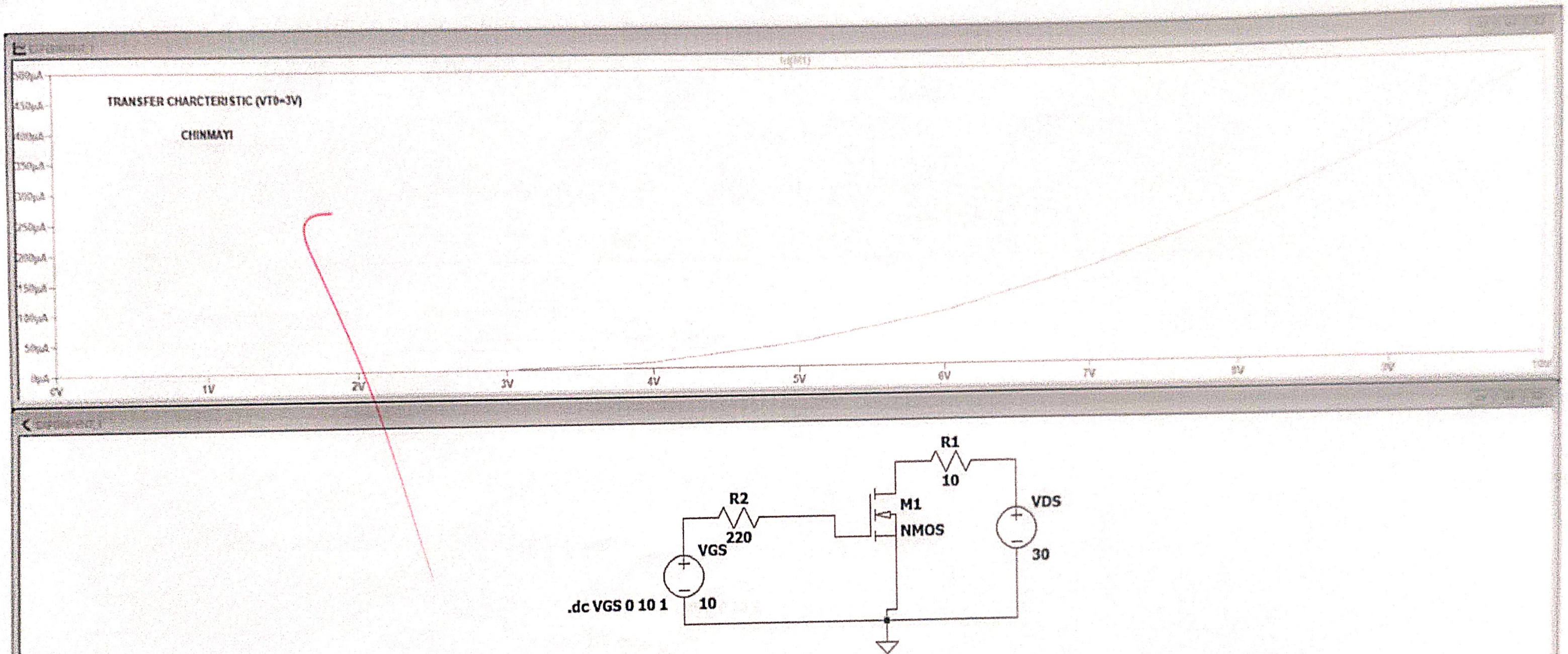


Figure 4. Transfer characteristics (VTO = 3V)

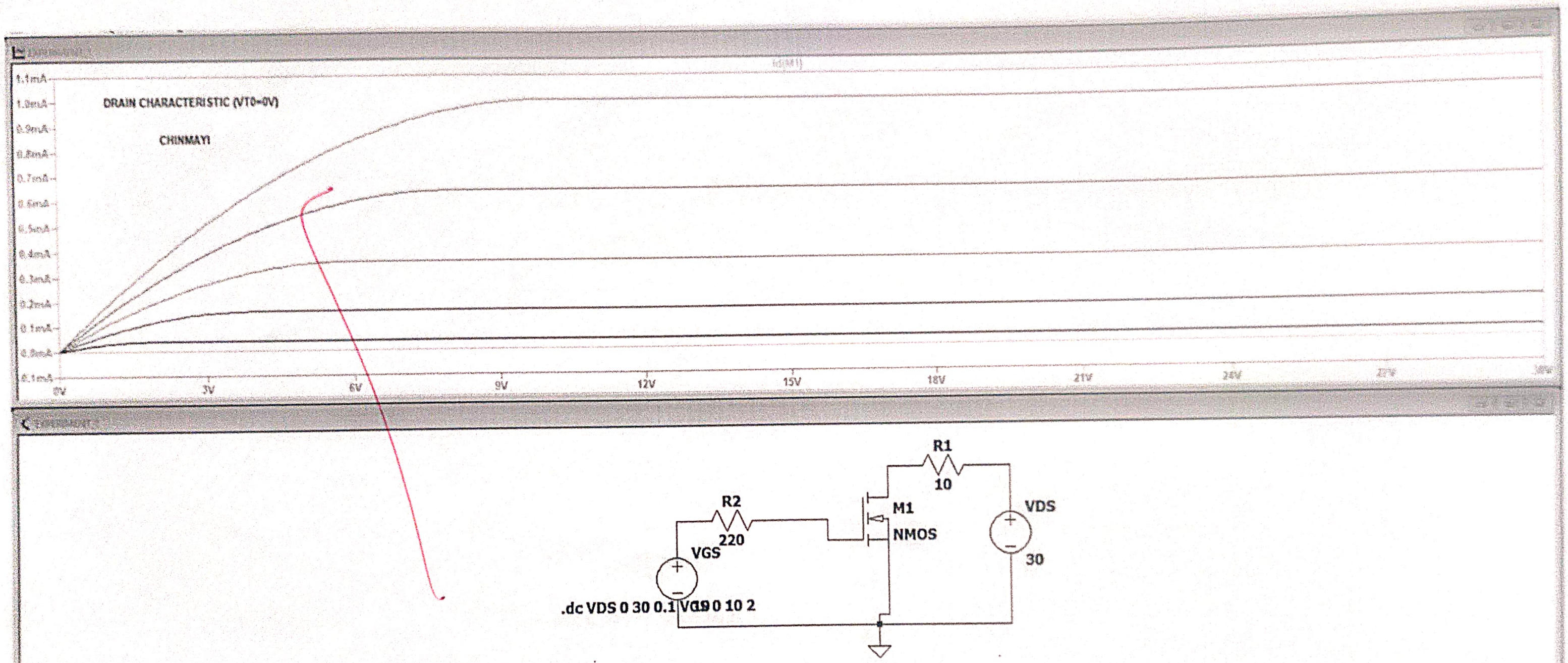


Figure 5. Drain Characteristic (VTo = 0V)

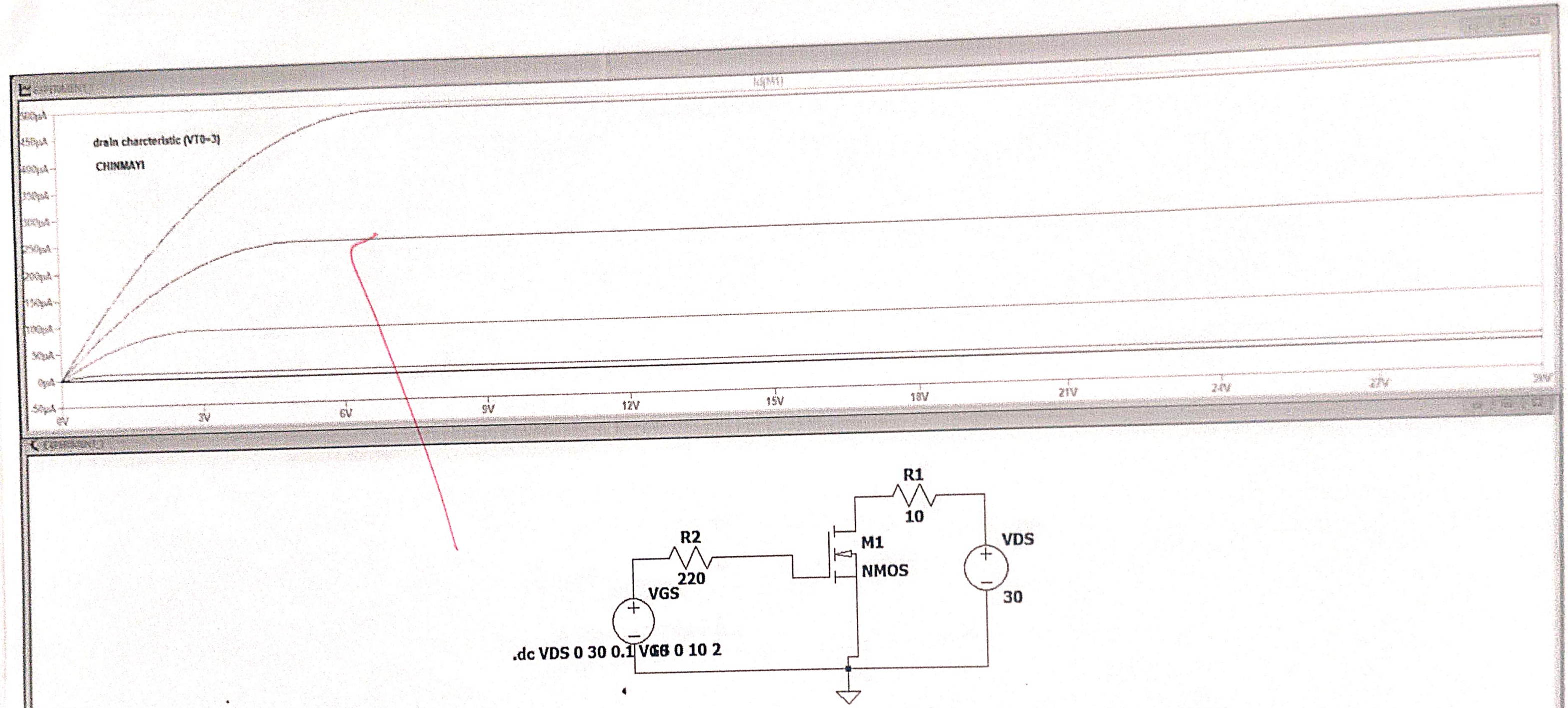
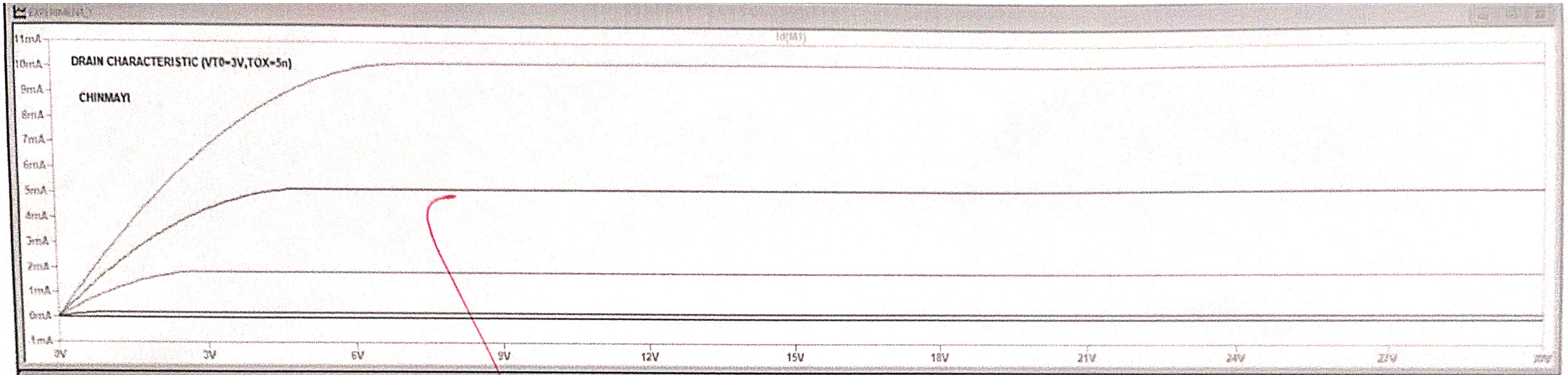


Figure 6. Drain characteristic ($V_{TO}=3$)



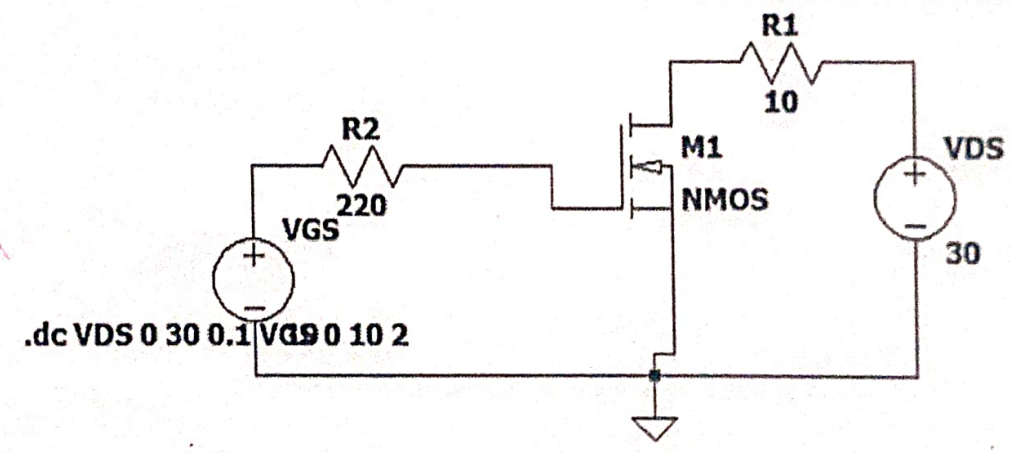


Figure 7. Drain characteristics (tox=5nm)

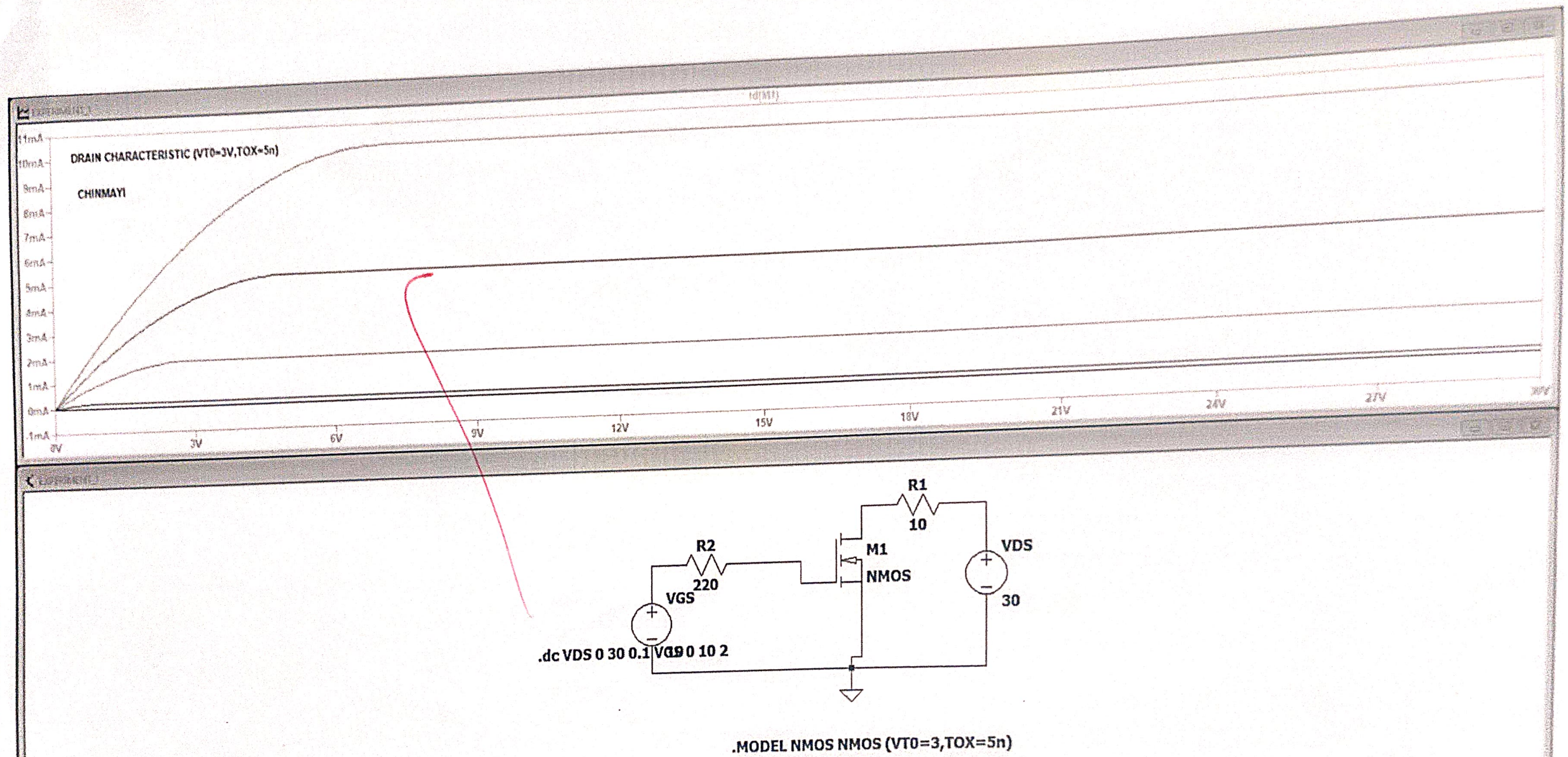
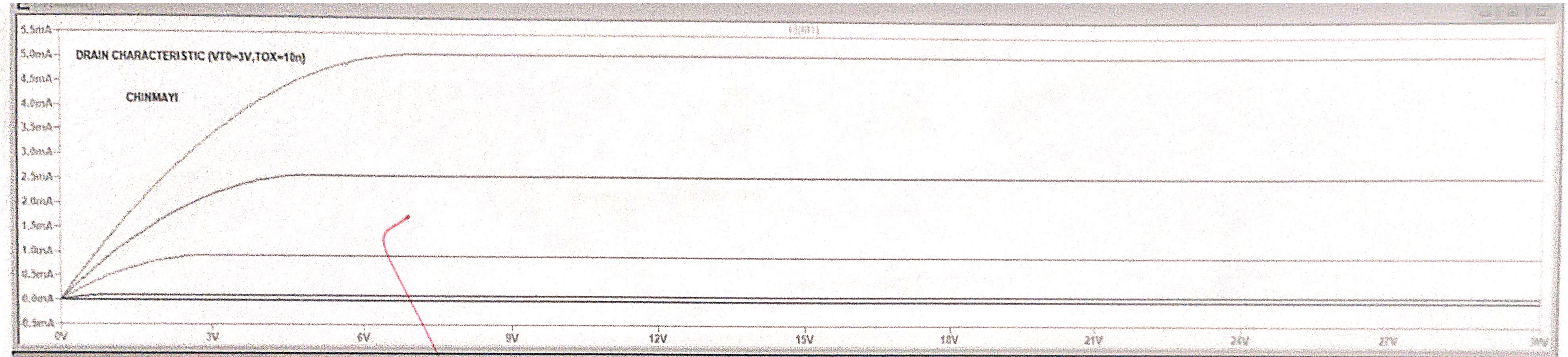


Figure 7. Drain characteristics (tox=5nm)



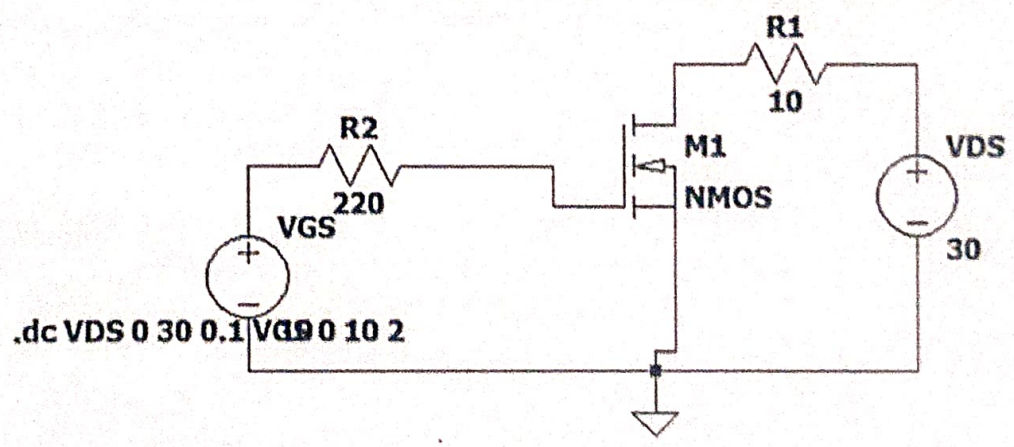


Figure 8. Drain characteristics (tox = 10nm)

$V_{GS} = 10V, V_T = 3V$

$$I_D = \frac{\mu_n C_{ox}}{2} \times \frac{W}{L} (V_{GS} - V_T)^2$$

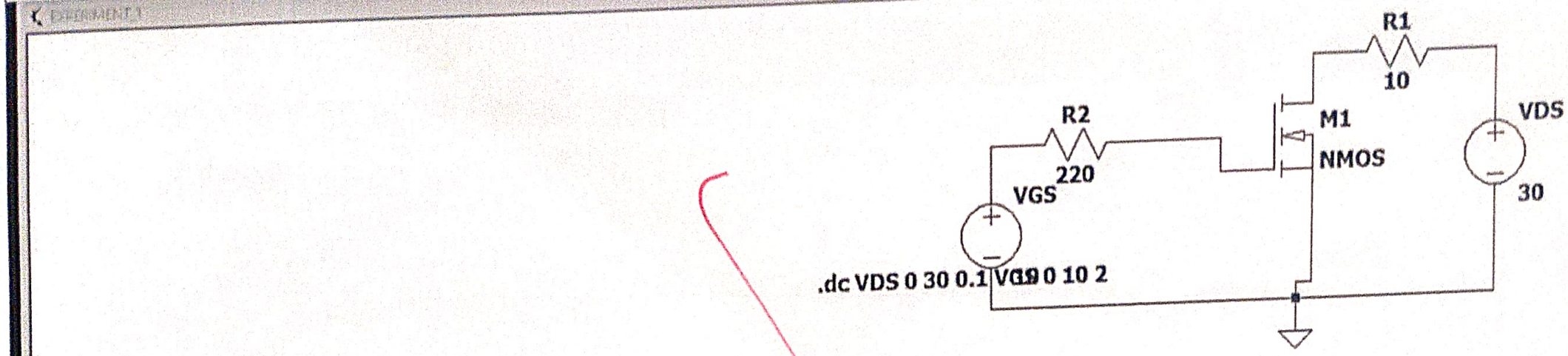
$$I_D = \frac{K_p}{2} (V_{GS} - V_T)^2 \quad (\text{let } K_p = 90\mu)$$

$$I_D = \frac{90 \times 10^{-6}}{2} (10 - 3)^2$$

$$I_D = 45 \times 10^{-6} (7)^2$$

I_D (theory) $= 2.205mA$

I_D (practical) $= 2.204mA$ ... (from graph)



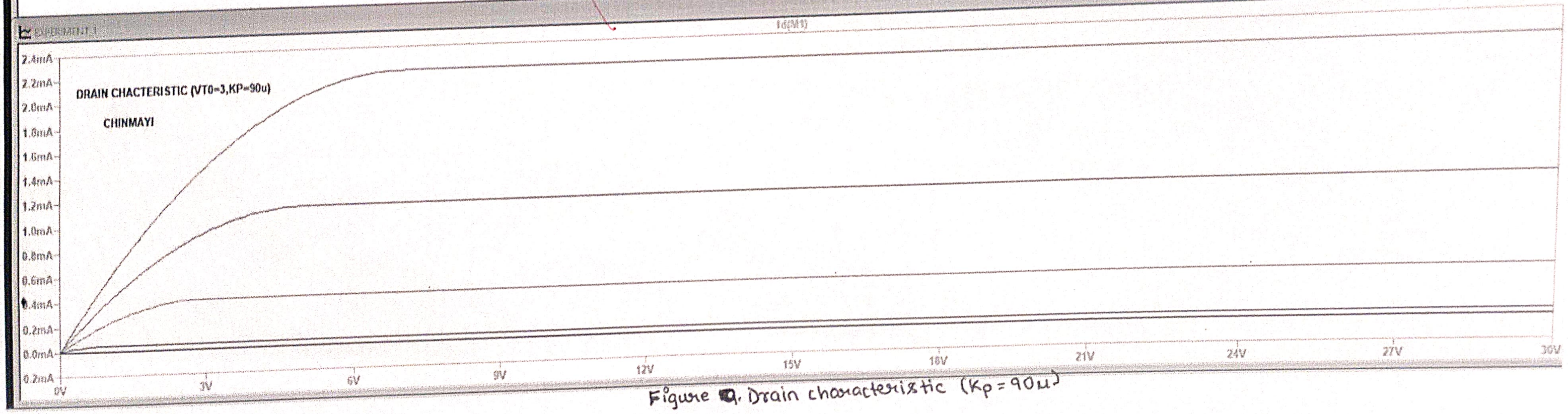
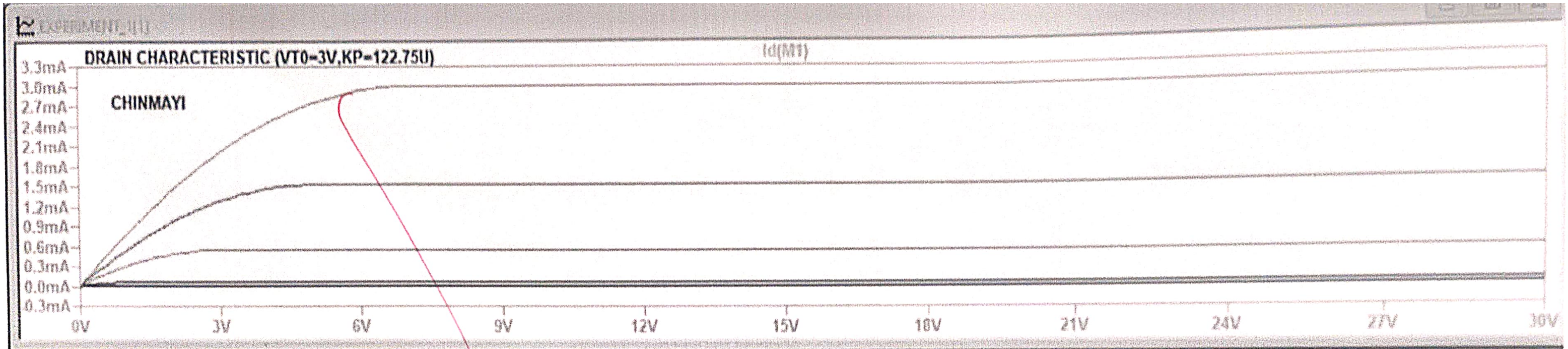


Figure 9. Drain characteristic ($K_p = 90\mu$)



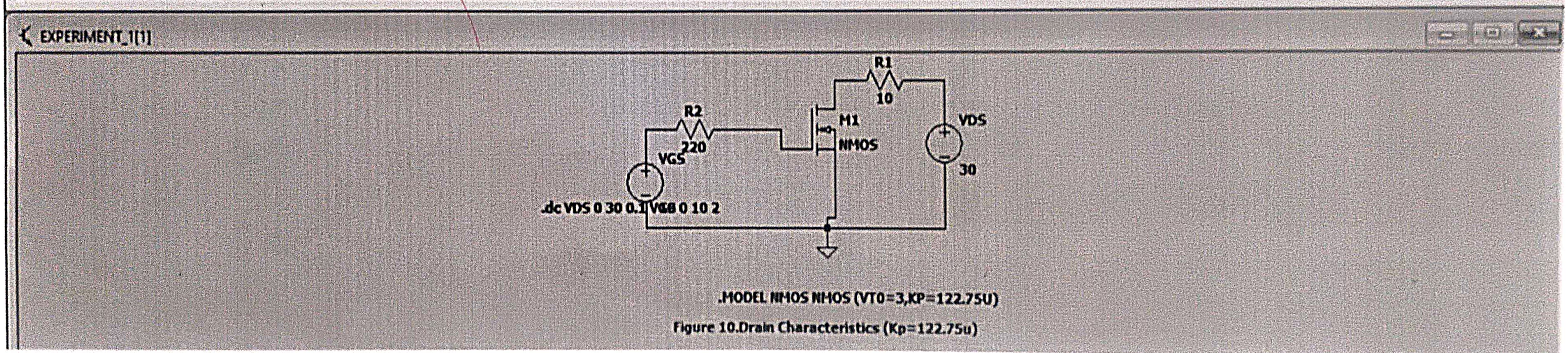


Figure 10.Drain Characteristics (Kp=122.75u)

Result analysis & Conclusion:

In this experiment, the drain and transfer characteristics of MOSFET based on Threshold voltage (V_T), Process Trans conductance (K_p) and channel length modulation parameter here we have observed if parameter like V_t, tox & kp changes have effect on I_D current: for eg: ① till $V_{GS} < V_T$ $I_D = 0$ but when $V_{GS} > V_T$, I_D current also increases,

② for tox - thickness of oxide is inversely proportional to I_D current has $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ & $I_D = \frac{\mu_n C_{ox}}{2} \times \frac{W}{L} (V_{GS} - V_T)^2$

∴ tox increases I_D decreases if tox decreases, I_D increases

③ for $k_p = \mu_n C_{ox} \times \frac{W}{L}$ has k_p is directly proportional to I_D current as $I_D = \frac{\mu_n C_{ox}}{2} \times \frac{W}{L} (V_{GS} - V_T)^2$.

∴ $k_p \uparrow$ $I_D \uparrow$ & $k_p \downarrow$ $I_D \downarrow$.

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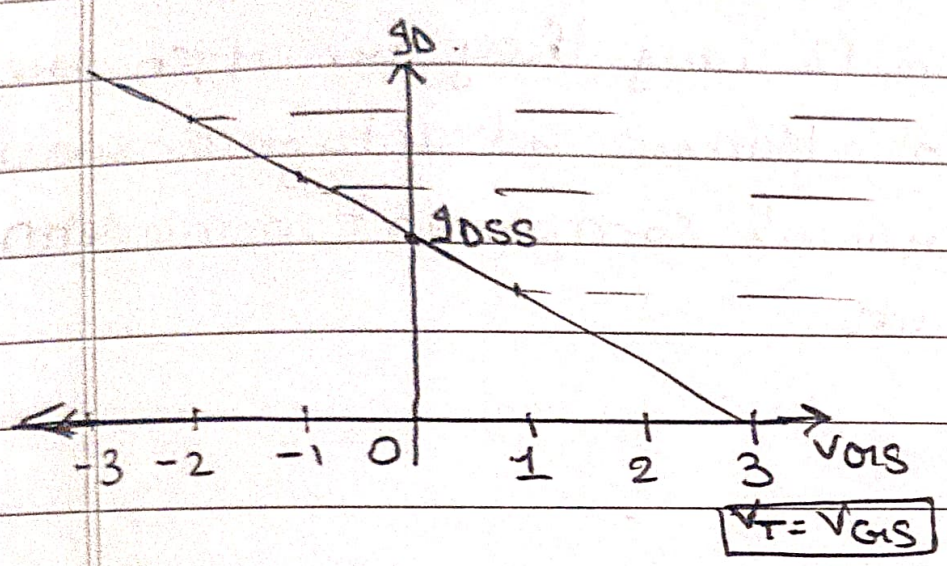
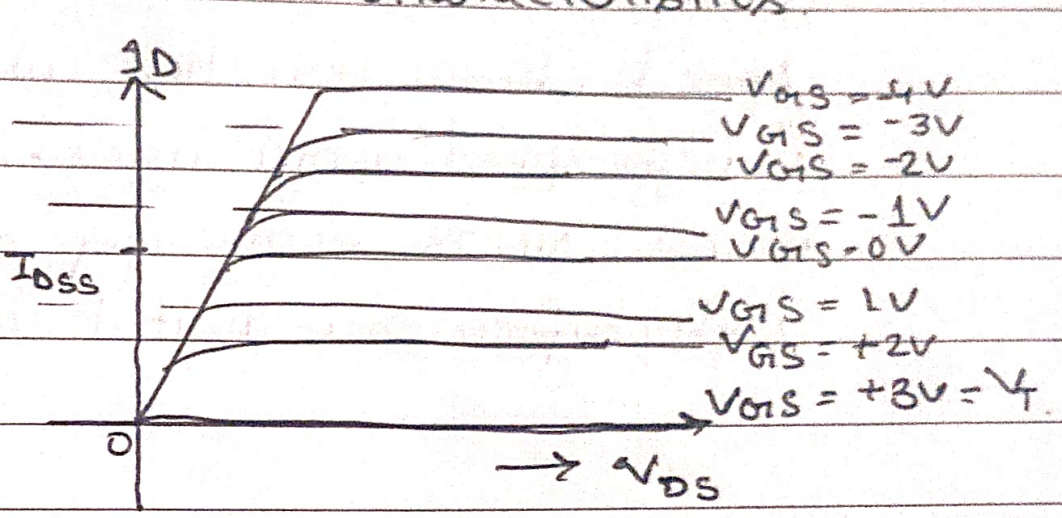
Resu Post Experiment Questions.

Q1] Draw characteristics of PMOSFET and write drain current equations.

→ Transfer characteristics



Drain Characteristics



Drain Current equations for PMOSFET.

$$I_{D(linear)} = \frac{\mu_p \cdot C_{ox}}{2} \times \frac{W}{L} \left[2 (V_{GS} - V_T) V_{DS} - V_{DS}^2 \right]$$

$$I_{D(saturation)} = \frac{\mu_p \cdot C_{ox}}{2} \times \frac{W}{L} (V_{GS} - V_T)^2$$

here μ_p = mobility of holes

C_{ox} = oxide capacitance

W = width of the channel

L = length of the channel

Q2] Explain whether PMOS transistors are faster than NMOS transistors and justify your answer.

→ NMOS transistors are generally faster than PMOS transistors. This speed difference arises due to the differences in the mobility of charge carries in the two types of transistors. NMOS transistors

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLST

Name of Student:	Chinmayi Umesh Upadhya
Roll No. :	48
Practical No.:	03
Title of Practical:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	04
Journal work and timely submission	10	9
Total	20	18

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

Checked by

Name of Faculty: S. Ichake

Signature:

Date: 6/8/24

Name:-Chinmayi Umesh Upadhya
Roll no 848

Vidyavardhini's College of Engineering & Technology

Department of Electronics & Telecommunication Engineering

Experiment No. 3

Aim: To plot drain characteristics of MOSFET and observe Channel length modulation effect.

Software: - LTspice software.

Theory:

Channel length modulation (CLM) is a phenomenon in MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) where the effective length of the transistor's channel decreases as the drain-to-source voltage (V_{DS}) increases. This effect occurs because a higher V_{DS} reduces the length of the depletion region near the drain, effectively shortening the channel. As V_{DS} increases, the channel becomes shorter, leading to an increase in drain current (I_D) even if the gate-to-source voltage (V_{GS}) remains constant as shown in figure 1. This deviation from the ideal behaviour (where I_D is independent of V_{DS} in saturation) is modelled by modifying the drain current equation to include a factor called channel length modulation factor (λ) that accounts for CLM as given by equation 1. The modified equation is:

$$I_D(Saturation) = \frac{1}{2}\mu nCox\frac{W}{L}\left(V_{GS} - V_T\right)^2(1 + \lambda V_{DS}) \qquad (1)$$

Channel-length modulation factor (λ) is important because it decides the MOSFET output resistance. The resistance of the channel is inversely proportional to its width-to-length ratio; reducing the length leads to decreased resistance and hence higher current flow.

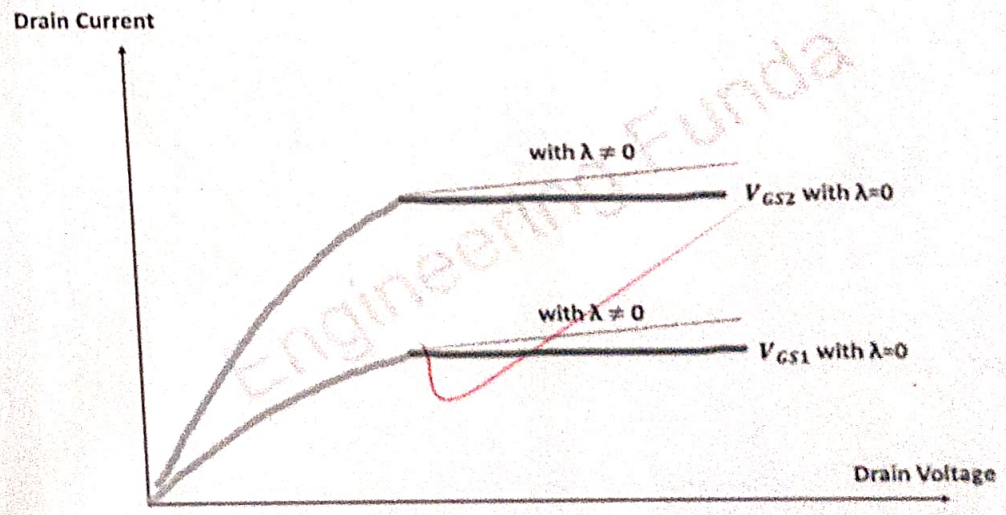


Figure 1. Drain Characteristics – Channel length Modulation

Procedure: -

1. Make new schematic.
2. Place component as per circuit diagram and connect it.
3. Select component values.
4. Select simulation profile as DC sweep.
5. Drain characteristics Vary VDS 0-30v in the step of 0.1V and VGS from 0 – 10V in the step of 2V. Plot drain characteristics.
6. Vary the value of Channel-length modulation factor (λ) and observe its effect on transfer characteristics and drain characteristics.

Calculation: I_D for $\lambda = 0$ (i.e No channel length modulation)

Let $K_p = 90\mu$, $V_{GS} = 10V$, $V_T = 2V$, $V_{DS} = 9$, $\lambda = 0$

$$I_{D(sat)} = \frac{K_p}{2}(V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$= \frac{90 \times 10^{-6}}{2}(10 - 2)^2 (1 + 0 \times 9)$$

$$= 45 \times 10^{-6} (64) \text{ (1)}$$

$I_{D\,theory} = 2.88\,mA$

$I_{D\,practical} = 2.88\,mA$

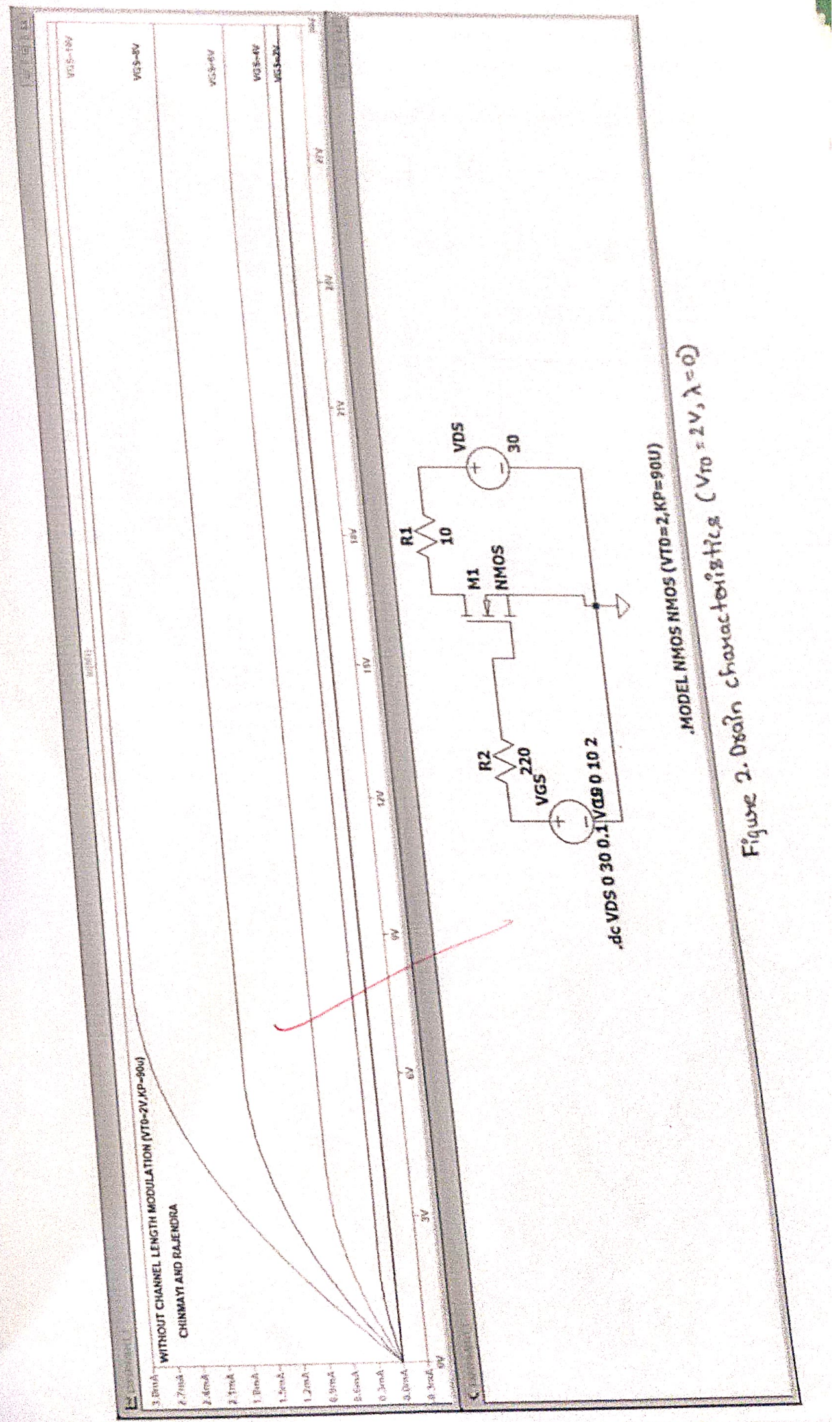


Figure 2. Drain characteristics

Calculation for Channel length modulation

for $K_p = 90\mu$, $V_{GS} = 10V$, $V_T = 2V$, $V_{DS} = 9V$, $\lambda = 0.04$

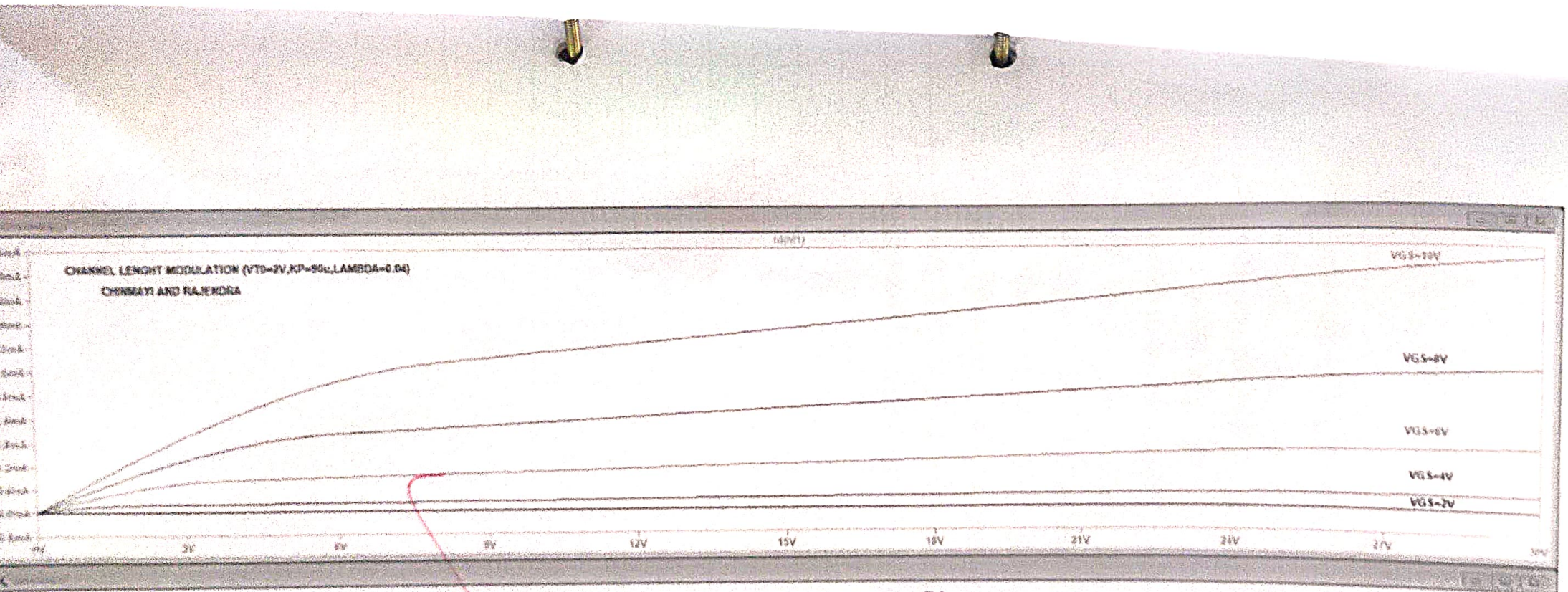
$$I_D(sat) = \frac{K_p}{2}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

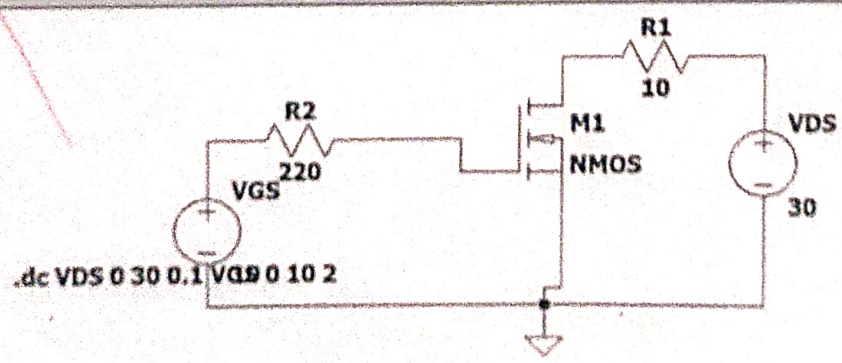
$$= \frac{90\times10^{-6}}{2}(10-2)^2(1+0.04\times9)$$

$$= 45\times10^{-6}(64)(1.36)$$

Io theory = 3.9168mA

I_D practical = 3.925mA





.MODEL NMOS NMOS (VTO=2,KP=90U,LAMBDA=0.04)

Figure 3. Drain characteristics ($V_{TO} = 2V$, $\lambda = 0.04$)

Result analysis and conclusion:

In this experiment, we have a observe channel length modulation effect with changes in value of channel length modulation factor (λ). when in saturation region $\lambda = 0$ means there is no channel length modulation means V_{DS} is constant for increase in V_{GS}. when in saturation region $\lambda \neq 0$ means there is channel length modulation that is V_{DS} increases with increase in V_{GS}. Has we have observe the I_D increases more with channel length modulation as the graph of drain characteristic, the slope increases in channel length modulation.

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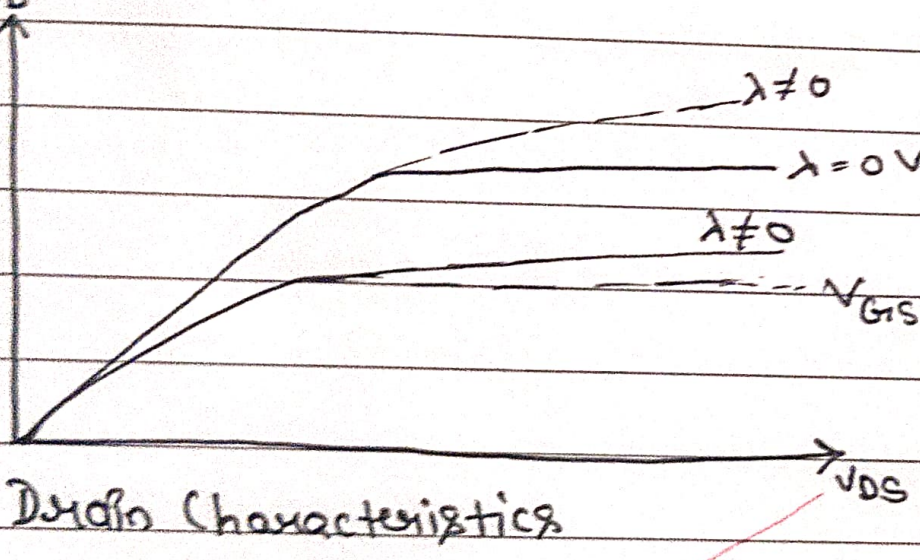
Post Experiment Question

Q.1] What is a significance of channel length modulation factor (λ)?

→ The channel length modulation factor (λ) is a crucial parameter in MOSFET (Metal oxide Semiconductor field effect transistor) design. It quantifies the variation in the channel length due to changes in the drain-source voltage V_{DS}, which in turn affects the drain current I_D. This phenomenon is similar to the Early effect in bipolar junction transistors. As depletion layer increases near the V_{DS}, still some current flows through the channel due to electric field present over there. As V_{DS} increases, the effective channel length decreases slightly, leading to an increase in I_D even in the saturation region. This non-ideal behaviour is captured by λ & is important for accurately modeling and predicting the performance of MOSFETs in analog & digital circuits, especially as device dimensions shrink in modern technologies.



Drain Characteristics

$$I_{D(sat)} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS})$$

here,

If $\lambda = 0$, there is no channel length modulation.

If $\lambda \neq 0$, there is channel length modulation.

Q2] Is there any effect of channel-length modulation on transfer characteristics, justify your answer.

→ Yes, As channel length modulation effects the drain current with increase in V_{GS} and V_{DS}, in transfer characteristic, where increase in V_{GS} after $V_{GS} > V_T$, I_D increases bcz channel is formed & more electron flow towards the channel which

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rapidly
increases the I_D current but after sometimes a depletion layer forms near the V_{DS} which decreases or the flows of current I_D thought I_D current increases little by little due to electric field it is not much but after channel length modulation, the I_D increases more with increase in V_{DS} as well as V_{DS} As I_D formula for Channel length modal after is given by $I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$
As λ increases I_D current also increases as it is directly proportional. Therefore, there is an effect of Channel length modulation on transfer characteristics.

6/8/24 -09/10

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Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmay Umesh Upadhya
Roll No. :	48
Practical No.:	04
Title of Practical:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	05
Journal work and timely submission	10	9
Total	20	19

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

Checked by

Name of Faculty: S. Khan

Signature:

Date: 13/8/24

Name :-chinmayi umesh Upadhya
Roll no:-48

Vidyavardhini's College of Engineering & Technology
Department of Electronics & Telecommunication Engineering

Experiment No.4

Aim: To plot and observe drain current of MOSFET for different types of scaling.

Software:-LTspicesoftware.

Theory: The design of high-density chips in MOS VLSI (Very Large-Scale Integration) technology requires that the packing density of MOSFETs used in the circuits is as high as possible and, consequently, that the sizes of the transistors are as small as possible. The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as scaling. Scaling of MOSFET transistor is involved with systematic reduction of overall dimension of the device as allowed by available technology, while preserving the geometric ratios found in the larger devices. A constant scaling factor's' is introduced. The scaled device is obtained by dividing all horizontal and vertical dimensions of the large size transistor by this scaling factor as shown in Table.1.

Table.1 Dimensions and voltages with and without scaling

Parameters	Before Scaling	After scaling	
		Full scaling	Constant Voltage scaling
Channel length	L	$L' = L/s$	$L' = L/s$
Channel width	W	$W' = W/s$	$W' = W/s$
Gate oxide thickness	tox	$tox' = tox/s$	$tox' = tox/s$
Junction depth	Xj	$Xj' = Xj/s$	$Xj' = Xj/s$
Power supply voltage	VDD	$VDD' = VDD/s$	$VDD' = VDD$
Threshold voltage	VT0	$VT0' = VT0/s$	$VT0' = VT0$
Doping densities	N_A, N_D	N_A',$N_D' = sN_A$, sN_D	N_A',$N_D' = s^2 N_A$, $s^2 N_D$
Oxide capacitance	Cox	$Cox' = Cox/s$	$Cox' = Cox/s$
Drain current	I_D	$I_D' = I_D/s$	$I_D' = s.I_D$
Power dissipation	P_D	$P_D' = P_D/s^2$	$P_D' = s.P_D$
Power density	P_D/Area	P_D/Area' = P_D/Area	P_D/Area' = s^3. P_D/Area

Advantages of scaling:

- Increases the switching speed.
- Reduces chip size.
- Reduces power dissipation.

Disadvantages of scaling:

- Short channel effect arises due to scaling which degrades the performance of MOSFET.

Types of scaling:

1.Full scaling/ Constant field scaling: The Full scaling technique attempts to preserve the magnitude of internal electric fields in the MOSFET, while the dimensions, power supply voltage & all terminal voltages are scaled down by factor of 's'. The peripheral and interface circuitry may require certain voltage levels for all inputs and output voltages, which in turn would necessitate multiple power supply voltages & complicated level – shifter arrangements. Hence for these reasons, constant voltage scaling is usually preferred over full scaling.

2. Constant voltage scaling: In Constant voltage scaling, all dimensions of the MOSFET are reduced by a factor of 's', but power supply & terminal voltage remain unchanged. In Constant voltage scaling, drain current density and power density are increased which may eventually cause serious reliability problem for the scaled transistor such as electro-migration, hot carrier degradation, oxide breakdown & electrical overstress.

Calculation:- (without scaling)

$K_p = 90\mu$, $V_{Th} = 3V$, $V_{GS} = 10V$, $V_{DS} = 30V$

① $I_D = \frac{K_p}{2}(V_{GS} - V_T)^2$

$= \frac{90 \times 10^{-6}}{2}(10-3)^2$

$= 45 \times 10^{-6}(7)^2$

$I_{theory} = 2.205\ mA$

$I_{practical} = 2.206\ mA$

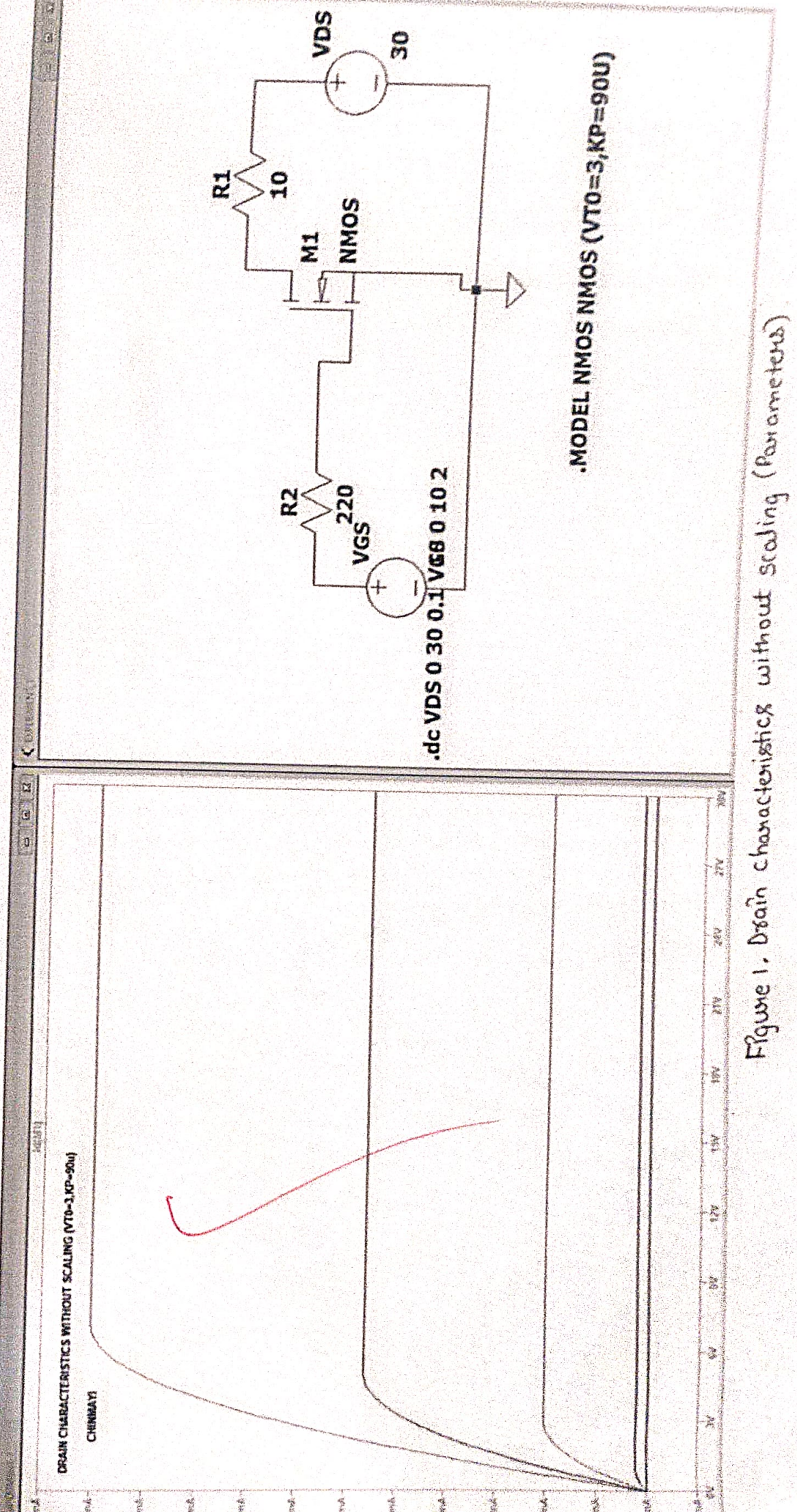

Figure 1, Drain characteristics without scaling (Parameters)

Calculation for with full scaling

s = 2

$I_D' = \frac{I_D}{s}$

$I_D' = \frac{2.205 \times 10^{-3}}{2}$

$I_{D\,theory}' = 1.1025\,mA$

$I_{D\,practical}' = 1.103\,mA$

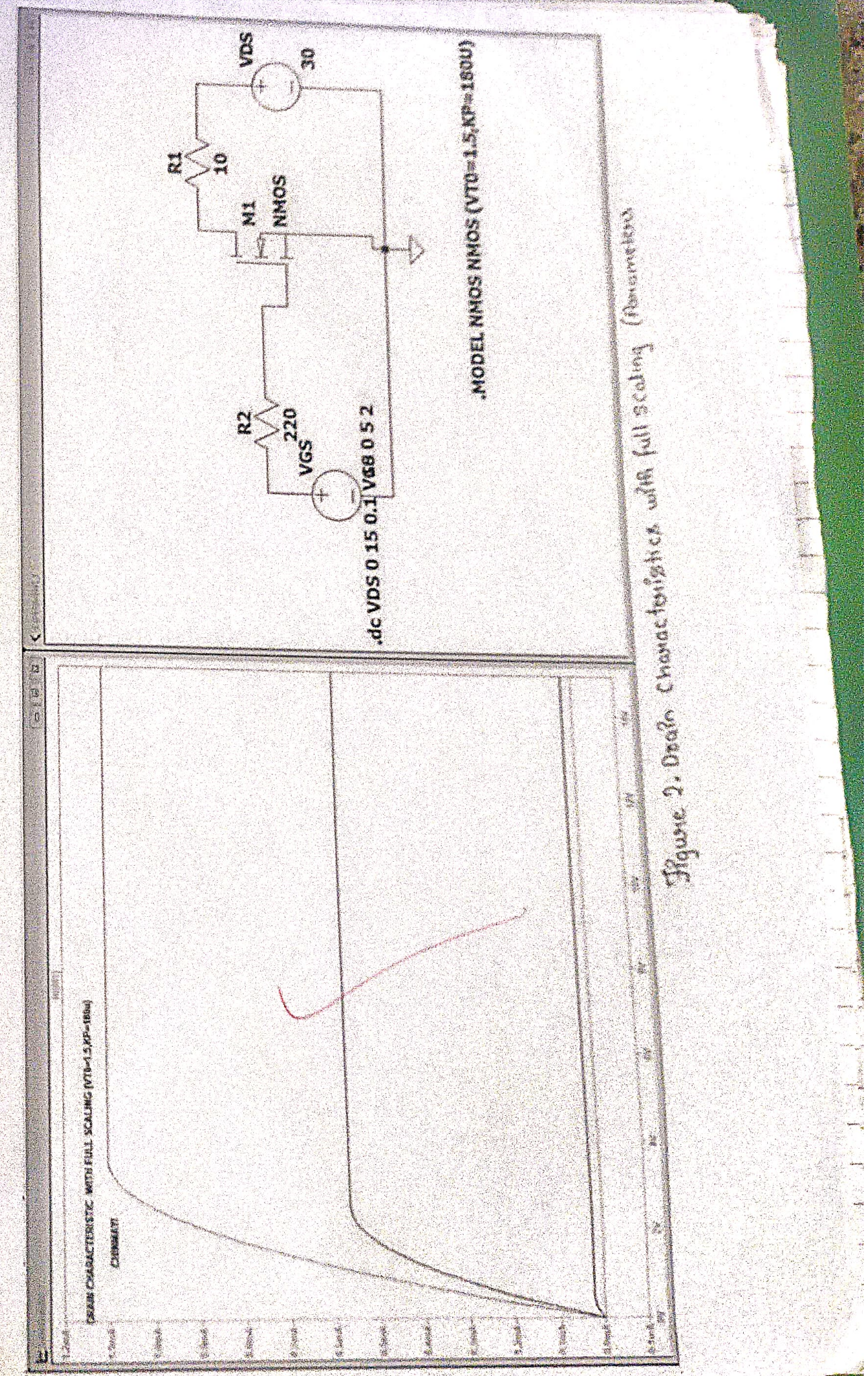

Figure 2. Drain Characteristics with full scaling (Nanometer)

Calculation

$I_D' = S I_D$

$I_D' = 2 \times 2.205 \times 10^{-3}$

I_D' theory = 4.41mA

I_D' practical = 4.412mA

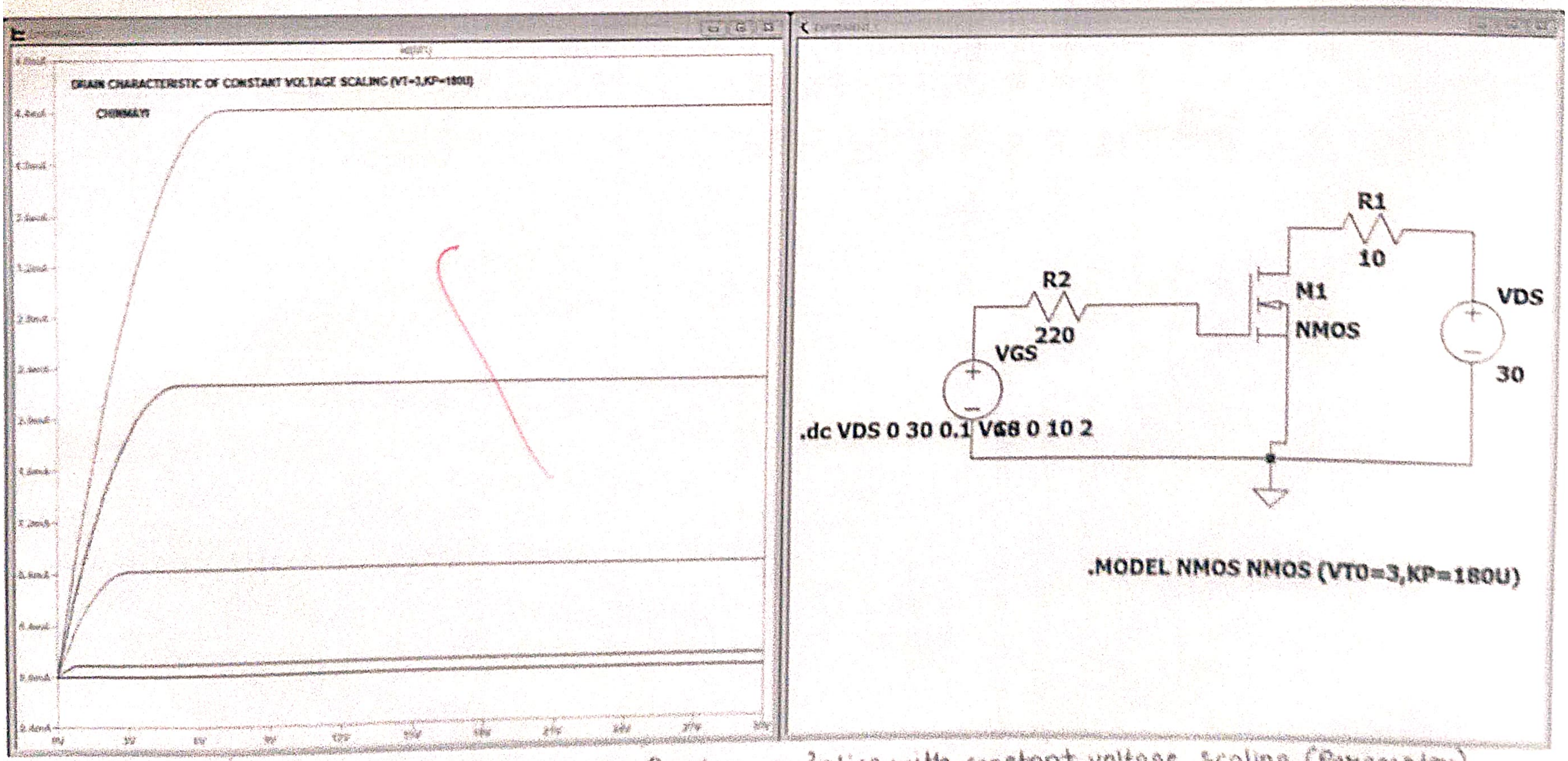

Figure 3. Drain characteristics with constant voltage scaling (Parameter)

Result analysis & Conclusion:-

In this experiment we have seen the effect of full-scaling where all dimension & voltage are reduced by s and the I_D current is reduced by s^2 but in constant voltage scaling only dimension are reduced by s factor leaving voltage constant. In full scaling we have observed the I_D current, current reduced where as in constant voltage current I_D increases by s factor.

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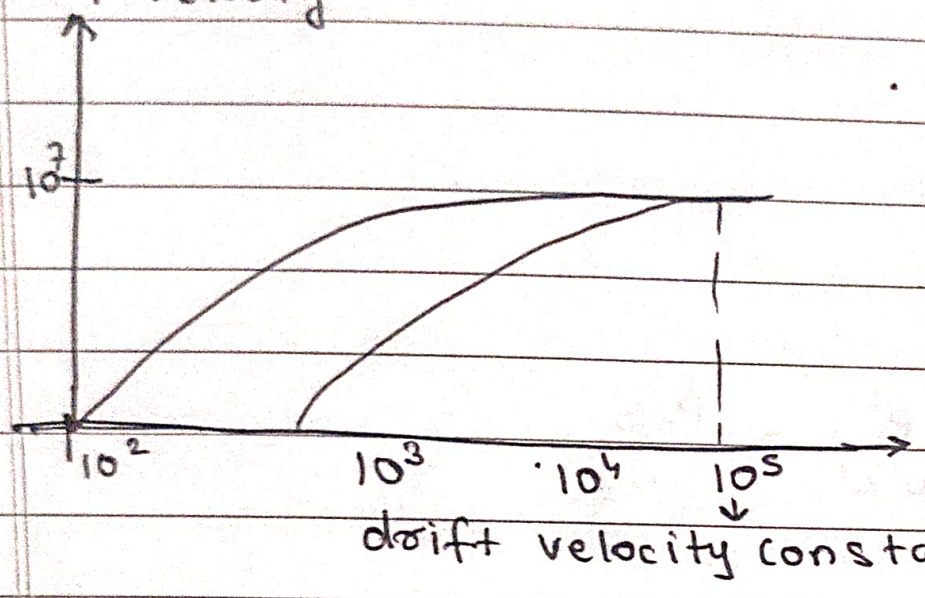
Post Experiment Questions:

Q1] Explain any one short channel effect.

→ There are 6 type of short Channel effect
1] Problem of Mobility Degradation.
2] Modification of threshold voltage
3] Drain induced barrier lowering
4] Drain punch through.
5] oxide breakdown
6] Impact Ionisation

① Mobility Degradation.



$V_d \propto E \rightarrow$ electric field

↓

drift velocity

$V_d = \mu_n E$

$\mu_n = \frac{V_d}{E}$

$\therefore \uparrow E = \frac{V\uparrow}{L\downarrow}$ Voltage applied increase, $L\downarrow \rightarrow$ length of channel decrease.

$\mu_n = \frac{V_d}{E} = \frac{10^7}{E\uparrow} \rightarrow$ Constant

$\therefore$ [(L) dimension ↓, E ↑, μ_n ↓, I_D ↓] → This is called mobility degradation

$\therefore I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2$

Q2] Prove that current in full scale devices is scaled by S.

→ $I_{D(linear)} = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (2(V_{GS} - V_T) V_{DS} - V_{DS}^2)$

$I_{D'(linear)} = \frac{k_D}{2} (2(V_{GS} - V_T) V_{DS} - V_{DS}^2)$

$I_{D'(linear)} = \frac{k_n'}{2} (2(V_{GS}' - V_T') V_{DS}' - V_{DS}^{2'})$

$= \frac{Sk_n}{2} \left(2\left(\frac{V_{GS} - V_T}{S}\right)\frac{V_{DS}}{S} - \frac{V_{DS}^2}{S^2}\right)$

$= \frac{1}{S} \frac{k_n}{2} (2(V_{GS} - V_T) V_{DS} - V_{DS}^2)$

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$I_{D'(linear)} = \frac{I_D(linear)}{S}$

Q3) Prove that power density for constant voltage is scaled up by S^3

→ $P = V_{DS} \cdot I_D$

$P' = V_{DS}' \cdot I_D'$

$P' = V_{DS} \cdot S I_D$

$P' = S(V_{DS} \cdot I_D)$

$P' = SP$

Power density $= \frac{P}{Area}$

Power density' $= \frac{P'}{Area'} = \frac{P'}{W'L'} = \frac{P \cdot S}{\frac{W}{S} \cdot \frac{L}{S}}$

$= S^3 \cdot \frac{P}{area}$

∴ Power density' $= S^3$ power density

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmayi Umesh Upadhya
Roll No. :	48
Practical No.:	05
Title of Practical:	To plot transfer & transient characteristics of resistive load inverter
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	04
Journal work and timely submission	10	09
Total	20	18

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

Checked by

Name of Faculty: S. Ichare

Signature:

Date: 20/8/24.

Experiment No. -: 5

Aim: To plot transfer and transient characteristics of resistive load inverter.

Software: -LTspice software.

Theory: The basic structure of a resistive load inverter is shown in the figure.1 given below.

Here, enhancement type NMOS acts as the driver transistor. The load consists of a simple linear resistor R_L. The power supply of the circuit is V_{DD}, and the drain current I_D is equal to the load current I_R.

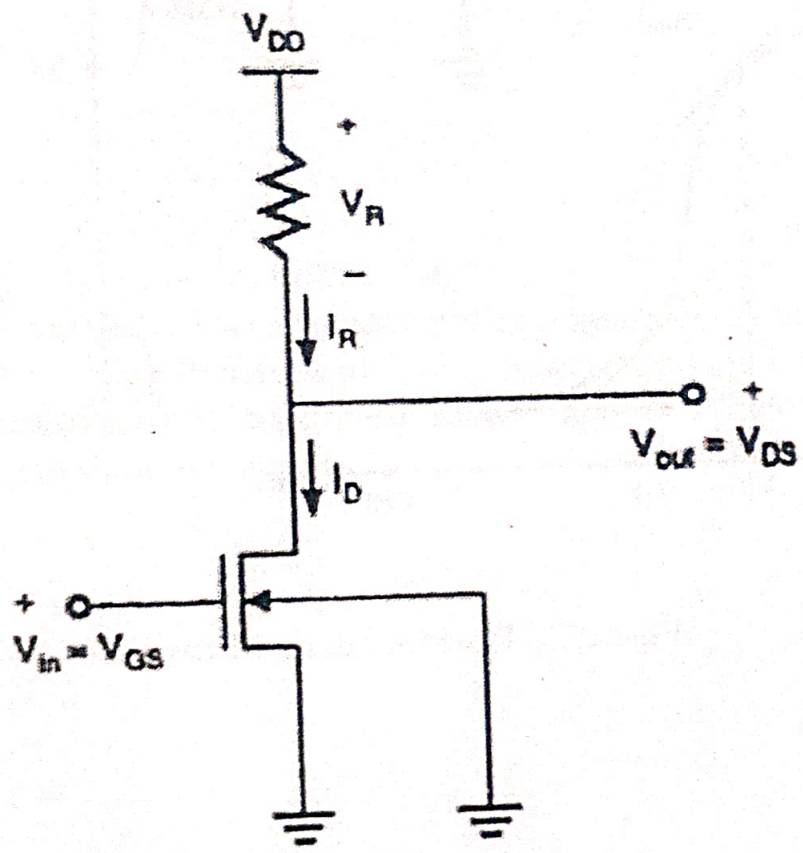


Fig.1.Resistive Load Inverter

When the input of the driver transistor is less than threshold voltage V_{TH} ($V_{in} < V_{TH}$), driver transistor is in the cut – off region and does not conduct any current. So, the voltage drop across the load resistor is ZERO and output voltage is equal to the V_{DD}

Noise Margin:

Noise margin is the amount of noise that a CMOS circuit could withstand without compromising the operation of circuit. Noise margin does makes sure that any signal which is logic '1' with

finite noise added to it, is still recognized as logic '1' and not logic '0'. It is basically the difference between signal value and the noise value. Transfer curve is shown in figure 2.

NM_L (NOISE MARGIN low) = VIL – VOL

NM_H (NOISE MARGIN high) = VOH – VIH

VIL = Low input voltage VIH = High input voltage

VOL = Low output voltage VOH = High output voltage

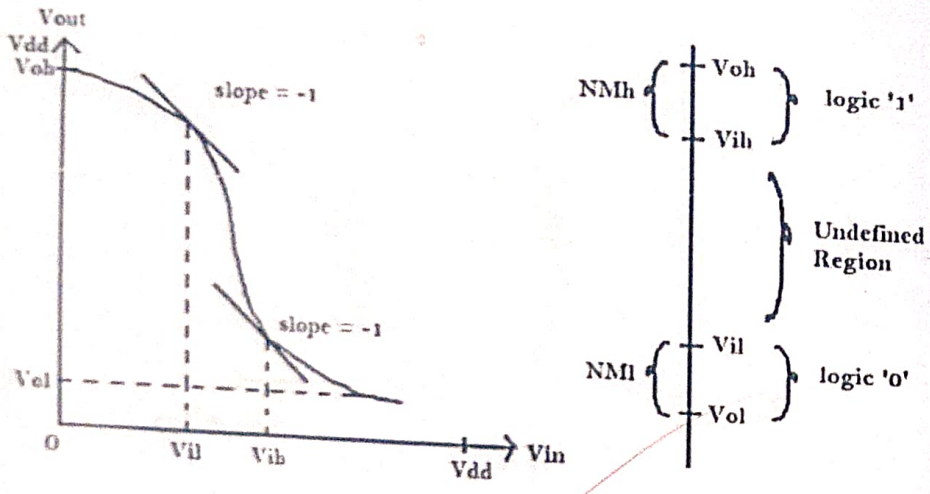
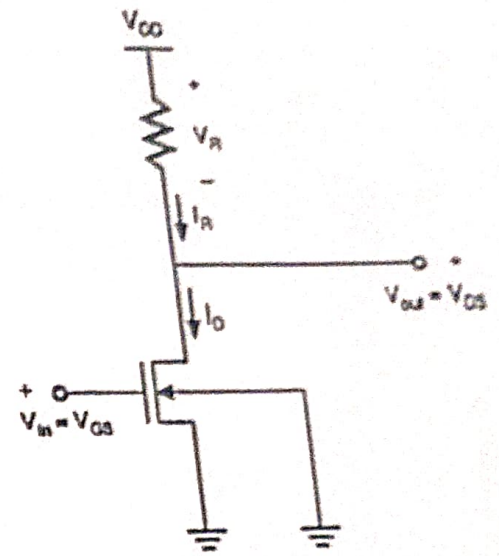


Figure 2. Transfer curve of inverter

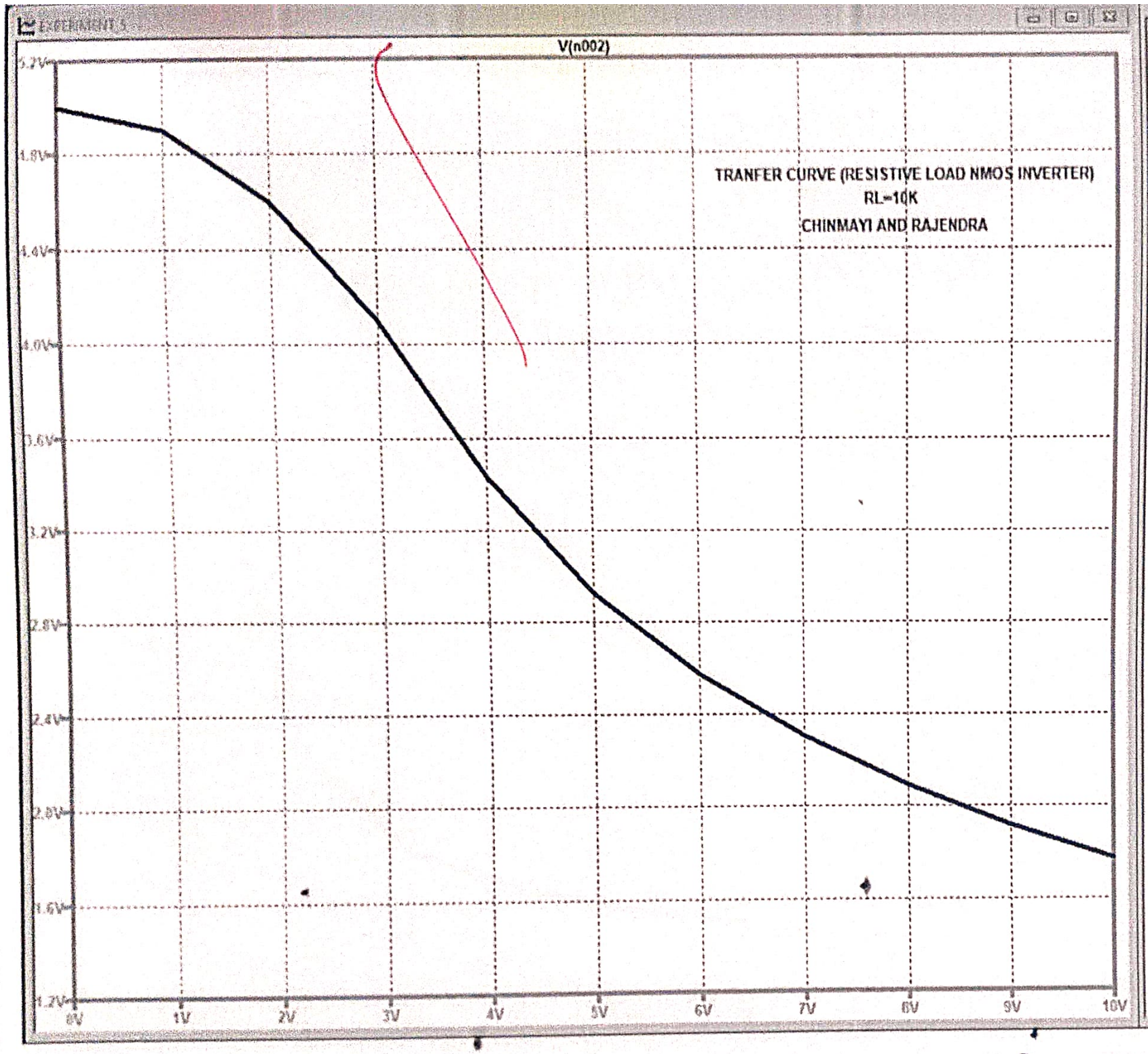
Circuit Diagram:



Procedure:

1. Draw the circuit in LT spice as per circuit diagram.
2. Plot voltage transfer curve by varying input voltage Vin from 0v to 3.3V.
3. Plot transfer curve for different values of R and observe voltage transfer curve.
4. Plot output waveform of inverter by giving Square input of 1 KHz and 3.3v.
5. Calculate noise margin from the graph.

Output Waveform:



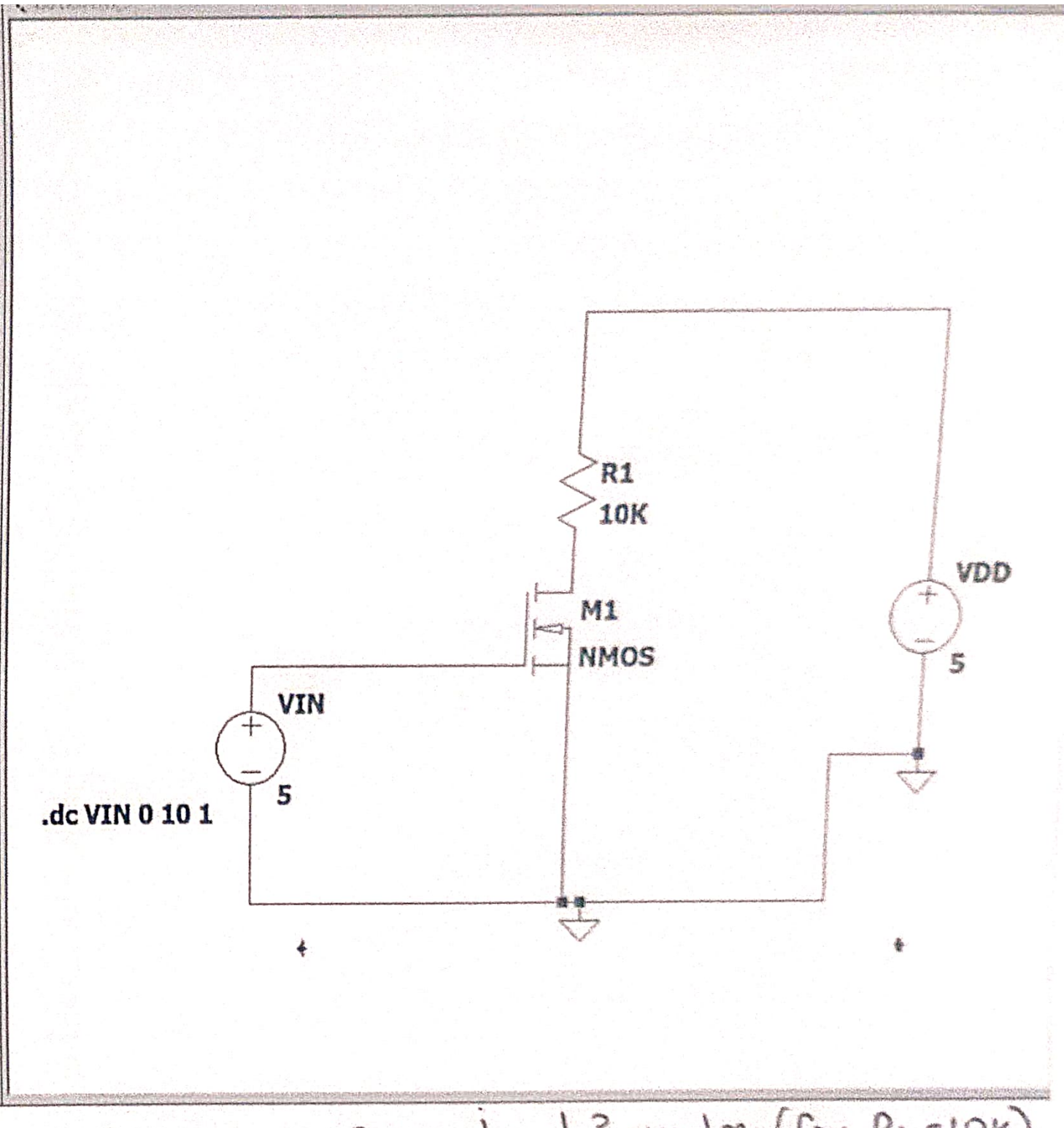
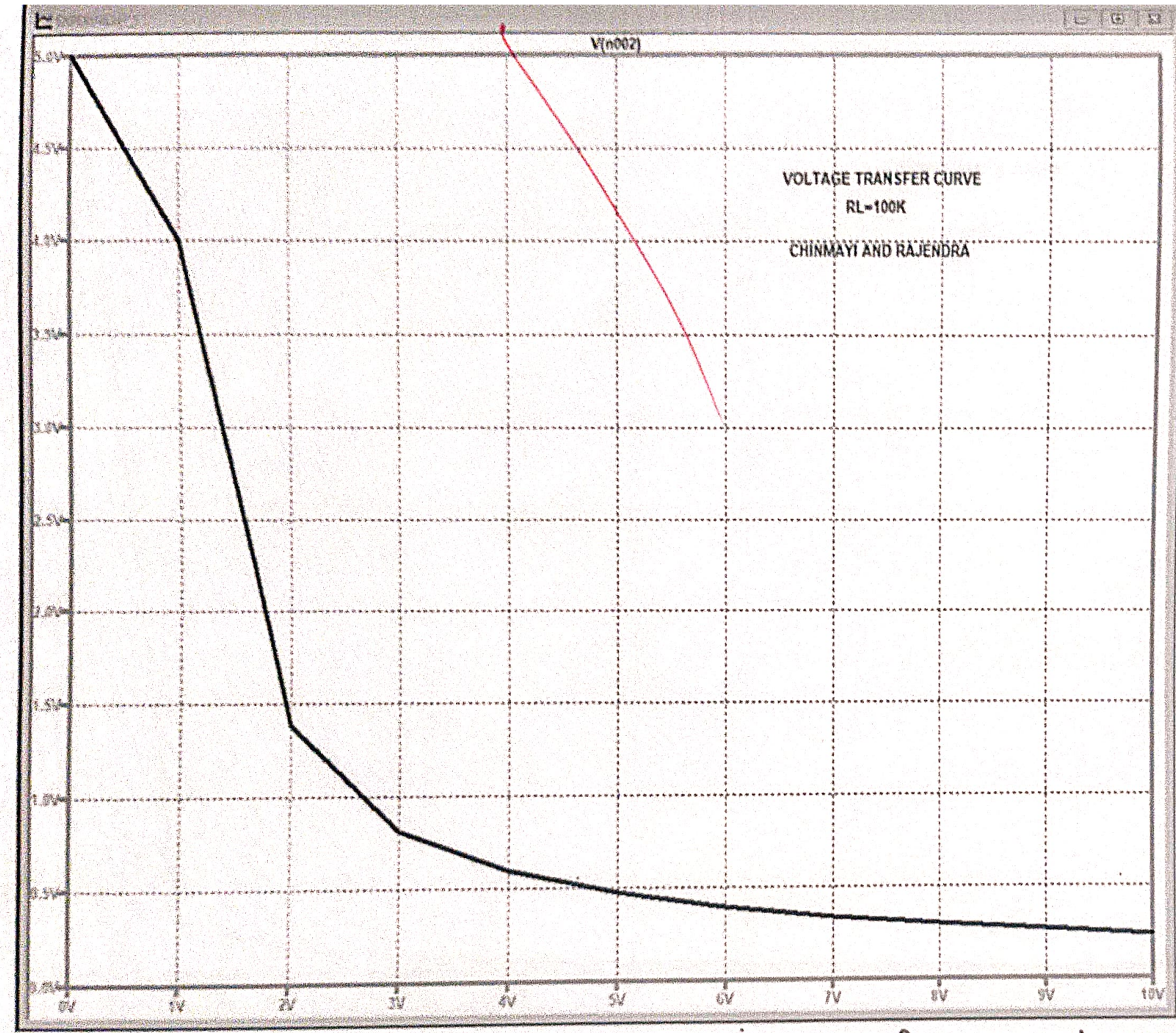


Figure 3.1. Transfer Curve of NMOS resistive load inverter (for R_L=10K)



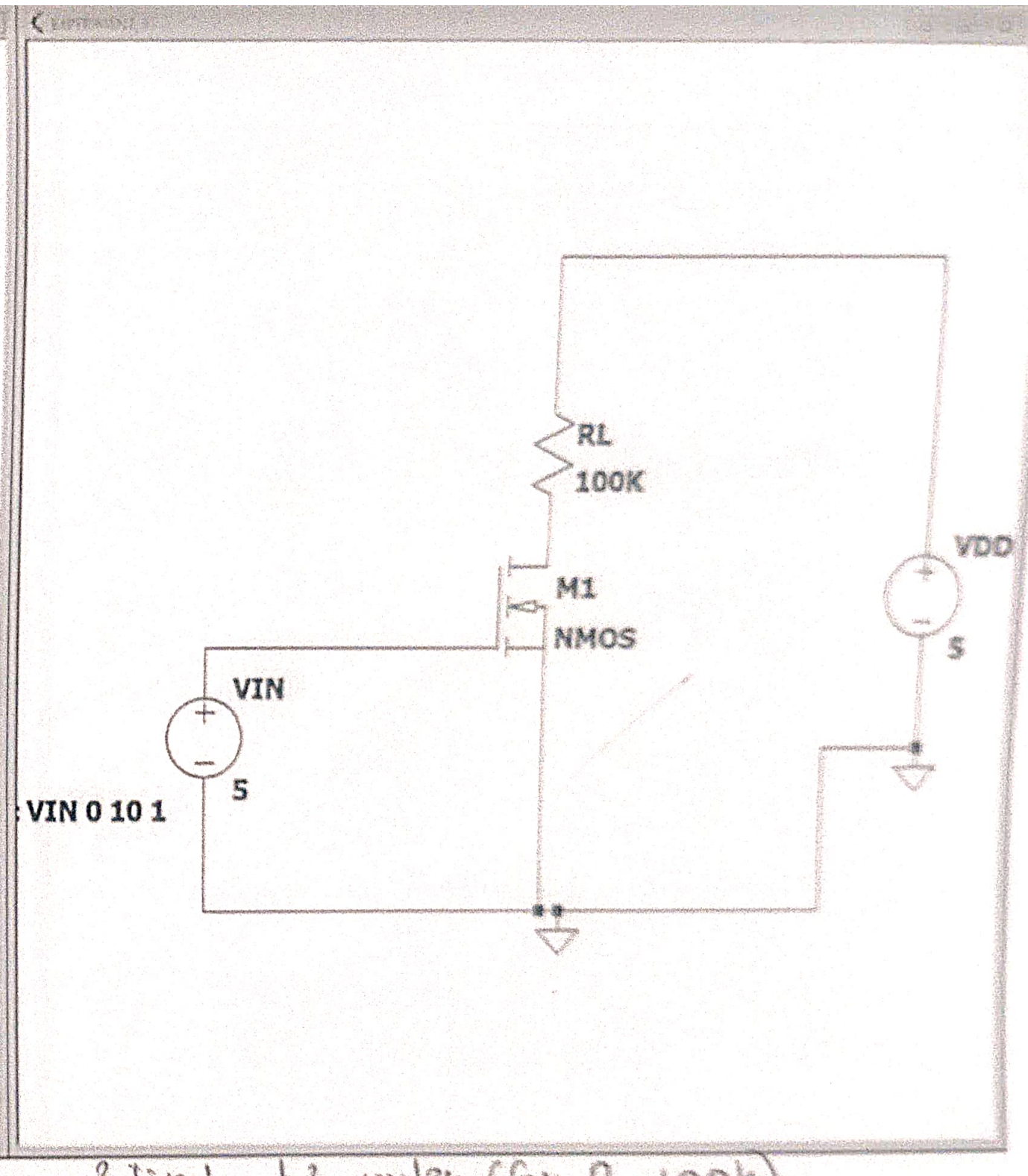
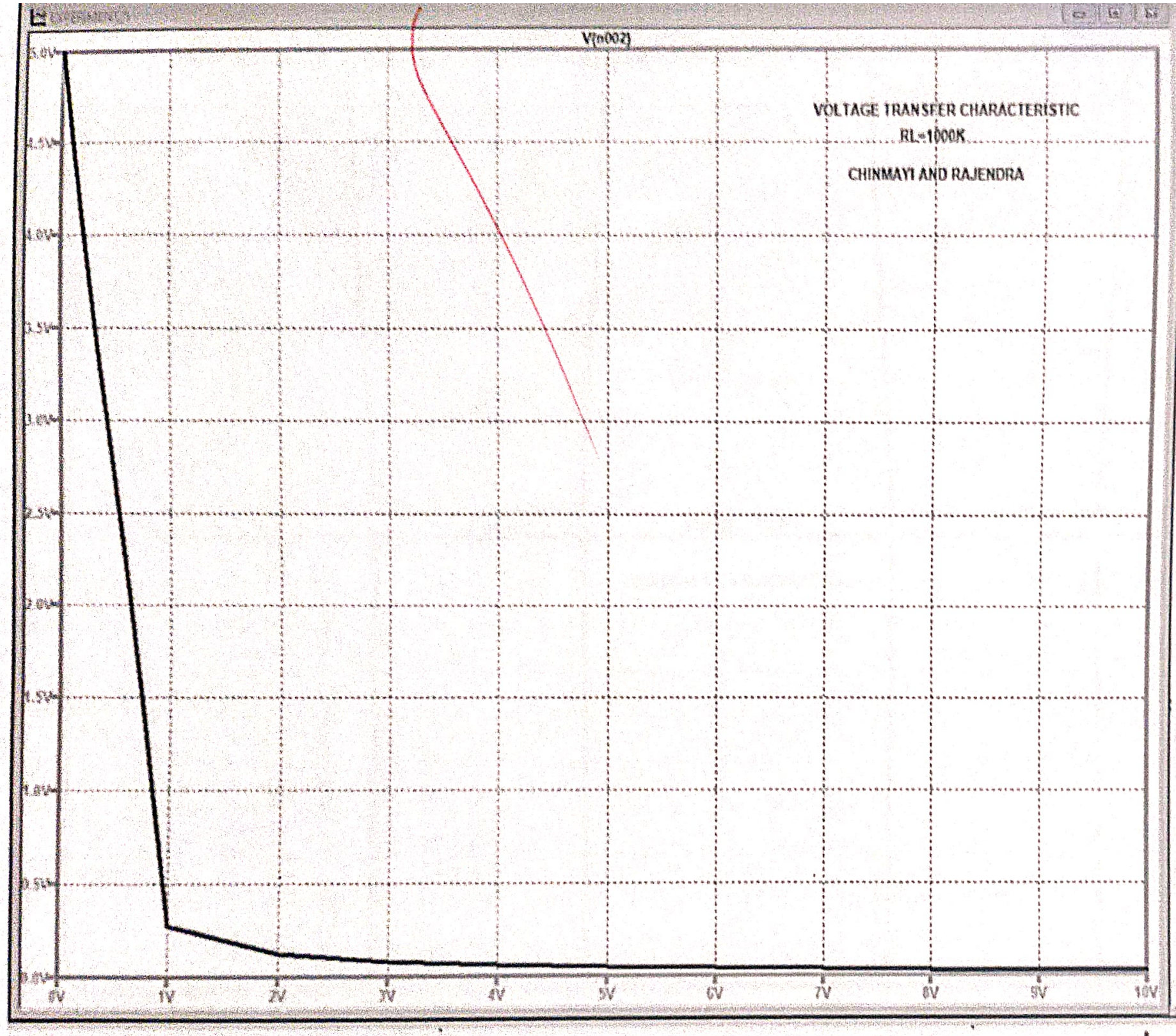


Figure 3.2. Transfer Curve of NMOS resistive load inverter (for R_L=100k)



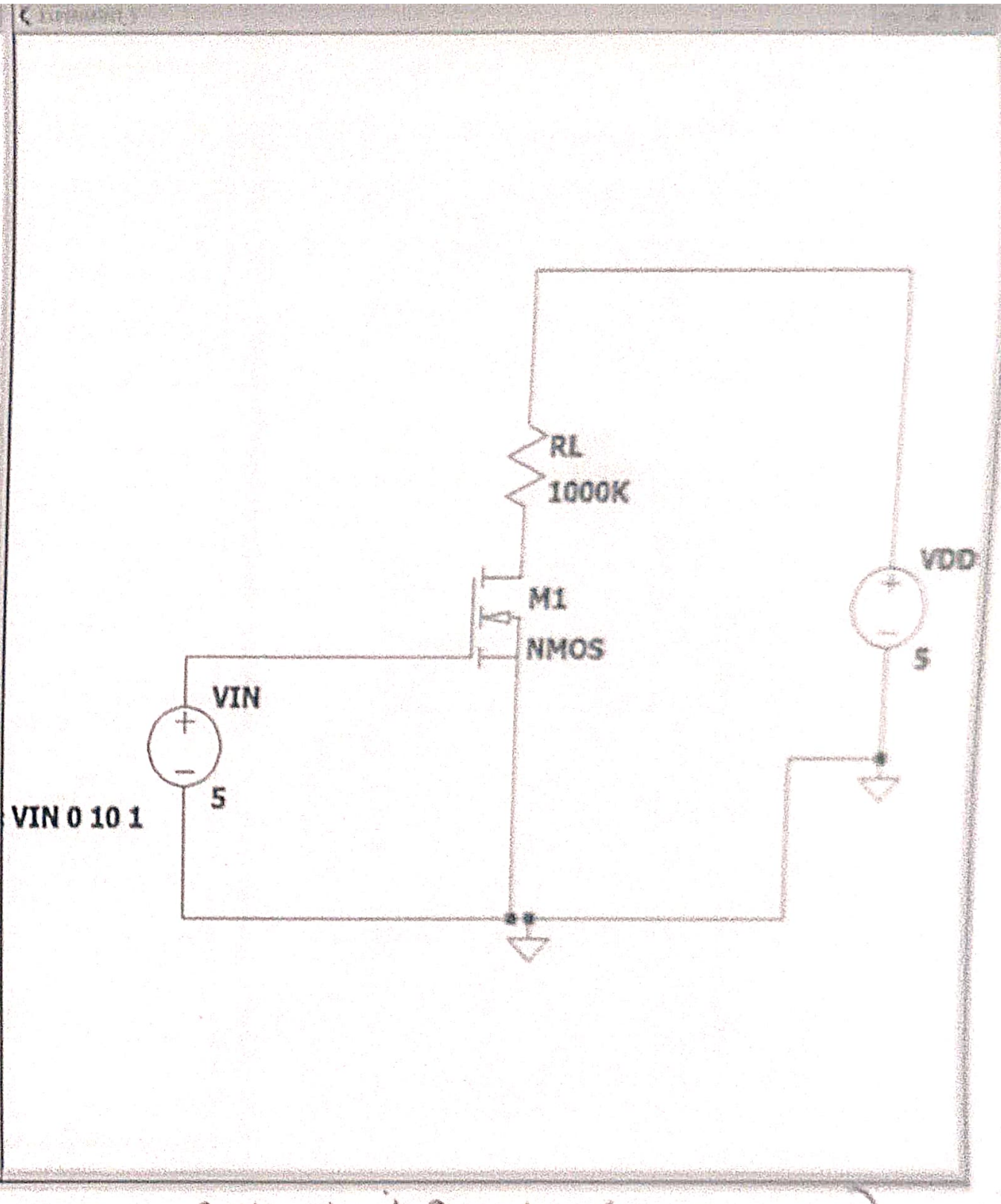


Figure 3.3. Transfer Curve of NMOS resistive load Inverter (for R_L=1000K)

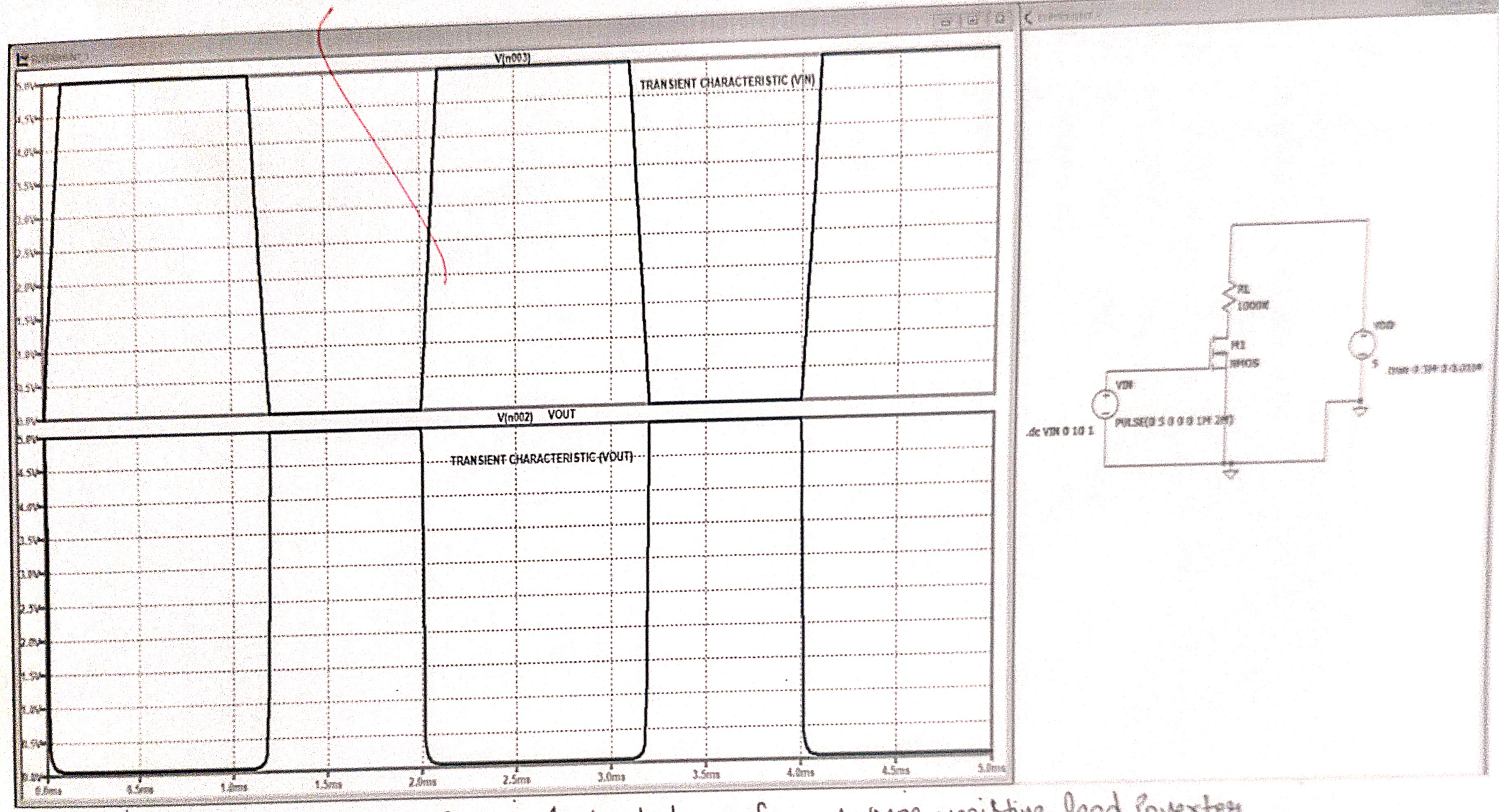


Figure 4 & Input output waveform of NMOS resistive load Inverter

Result analysis and Conclusion

In this experiment, we have observed that when resistor value increase the slope or curve also improves and almost it become like a ideal characteristic. In transient plot we have observed when input is high, output is low and when input is low, output is high. ~~Noise Margin of this graph~~ when we increase the RC value then it will take more area & more power consumption. In this experiment we have observed Vo by changing value of R_L from 10K, 100K & 1000K.

Post Experiment Question:-

Q1] How to improve noise margin of NMOS inverter with resistive load?

→ We can improve noise margin of NMOS inverter with resistive load by reducing the threshold voltage (V_{th}) of the nmos transistor, as it shifts the voltage transfer characteristics, allowing for better distinction between logic levels. Additionally increasing the resistive load's value can enhance the noise margin, as it makes the output voltage swing closer to the supply voltage when the NMOS is off, ensuring a clearer separation between logic '0' & logic '1'. Furthermore, adjusting the W/L ratio by increasing can reduce noise susceptibility and enhance overall noise margin.

Q2] what are the drawbacks of NMOS inverter with resistive load & how to overcome it?

→ Drawbacks of NMOS inverter with resistive load are:-

1] By increasing the value of RC will take more area & more power consumption.

2] Poor noise margins & limited o/p swing

To overcome these issue, replace the resistive load with an active load (like a pmos) Use a higher V_{DD} for better noise margins. These approaches reduce power loss, enhance speed and improve overall performance.

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmayi Umesh Upadhya
Roll No. :	48
Practical No.:	06
Title of Practical:	To plot voltage transfer & transient characteristics of CMOS inverter
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	04
Journal work and timely submission	10	09
Total	20	18

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

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Name of Faculty: S. Ichare

Signature:

Date: 03/09/24

Experiment No. 6

Aim: To plot voltage transfer and transient characteristics of CMOS inverter.

Software:-LTspice software.

Theory: Voltage transfer characteristics of CMOS inverter is a plot of input voltage and output voltage. Transfer characteristics is divided into five regions based on region of operation of PMOS and NMOS transistor. Transfer characteristics is shown in figure 1.

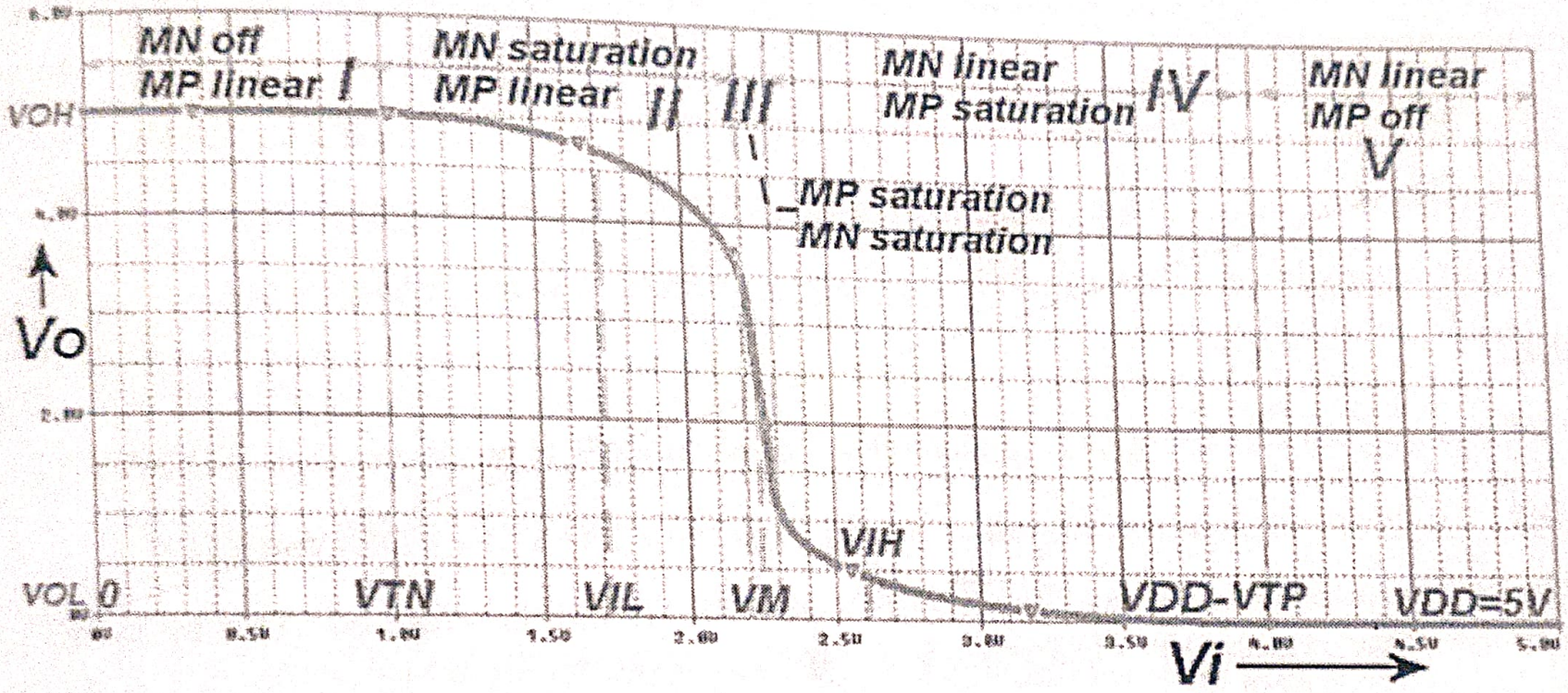

Figure 1. VTC of CMOS inverter

Region I:

In region I apply an input voltage between 0 and VTN.

- The PMOS device is forward biased (VSG > -VTP) and therefore on. This MOSFET is in the linear region (VSD<=VSG+VTP=VDD-Vo+VTP).
- The NMOS device is cut off since the input voltage is below VTN (Vi=VGS<VTN).
- The power dissipation is zero.

Region II

The input voltage is raised above VTN, the PMOS device remains in the linear region since it still has adequate forward bias. The NMOS turns on and jumps immediately into saturation since it still has a relatively large VDS across it.

- The PMOS device is in the linear region (VSD<=VSG+VTP).
- The NMOS device is in the saturation region (Vi=VDS>=VGS-VTN=Vo-VTN).
- Current now flows through both devices. Power dissipation is no longer zero.

The maximum allowable input voltage at the low logic state (VIL) occurs in this region. VIL is the value of Vi at the point where the slope of the VTC is -1. Put another way, VIL occurs at (dVo/dVi) =-1

Region III

In the middle of this region there exists a point where Vi=Vo. This point VM and identify it as the gate threshold voltage.

- The PMOS device is in the saturation region (VSD>=VSG+VTP=VDD-Vo+VTP).
- The NMOS device is in the saturation region (VDS>=VGS-VTN=Vo-VTN).
- Power dissipation reaches a peak in this region, namely at where VM=Vi=Vo.

Region IV

Region IV occurs between an input voltage slightly higher than VM but lower than VDD-VTP.

- The PMOS device is in the saturation region (VSD>=VSG+VTP=VDD-Vo+VTP).
- The NMOS device is forward biased (Vi=VGS > VTN) and therefore on. This MOSFET is in the linear region (Vi=VDS<=VGS-VTN=Vo-VTN).

The minimum allowable input voltage at the logic high state (VIH) occurs in this region. VIH occurs at the point where the slope of the VTC is –1 (dVo/dVi)=-1.

Region V

The NMOS device is forward biased (Vi=VGS > VTN) and therefore on. This MOSFET is in the linear region (Vi=VDS<=VGS-VTN).

- The PMOS device is cut off when the input is at VDD (VSG=0 V).
- The total power dissipation is zero just as in region I.
- For CMOS inverters, VOH=VDD. VOL is defined to be the output voltage of the inverter at an input voltage of VOH.

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Power Dissipation:

CMOS inverter dissipates a negligible amount of power during steady state operation. Power dissipation only occurs during switching and is very low. In figure 2 the maximum current flows, the on transistor supplies current to an output load if the output voltage deviates from 0 V or VDD. This makes CMOS technology useable in low power and high-density applications.

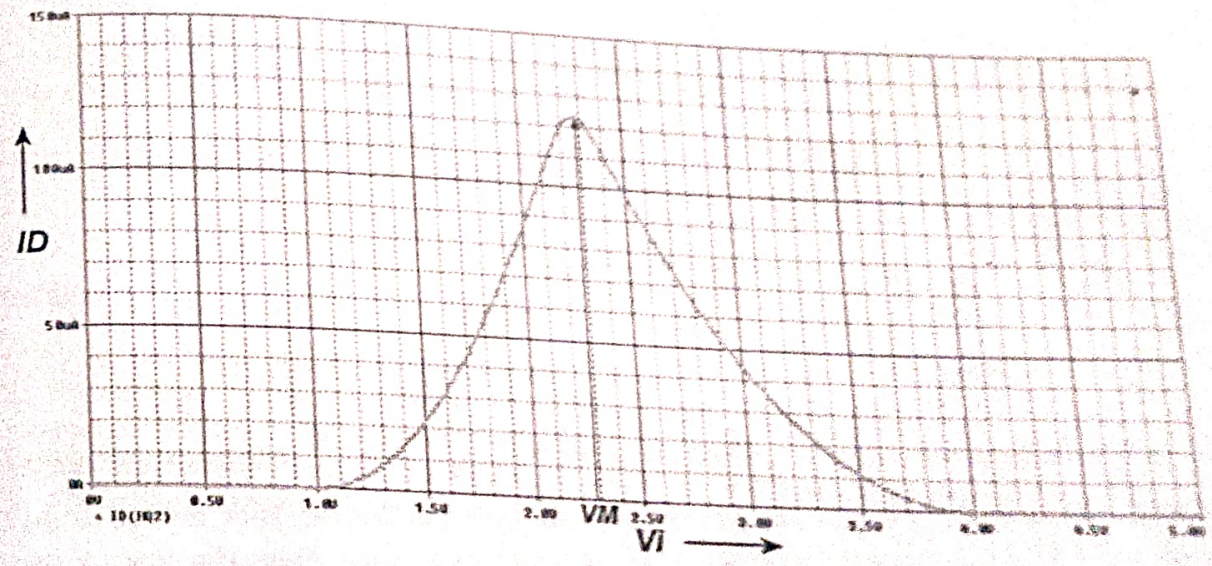


Figure 2 CMOS Inverter voltage and drain current graph

NOISE MARGIN:

Noise Margin:

Noise margin is the amount of noise that a CMOS circuit could withstand without compromising the operation of circuit. Noise margin does makes sure that any signal which is logic '1' with finite noise added to it, is still recognized as logic '1' and not logic '0'. It is basically the difference between signal value and the noise value as shown in figure.3.

NM_L (NOISE MARGIN low) = VIL – VOL

NM_H (NOISE MARGIN high) = VOH – VIH

VIL = Low input voltage VIH = High input voltage

VOL = Low output voltage VOH = High output voltage

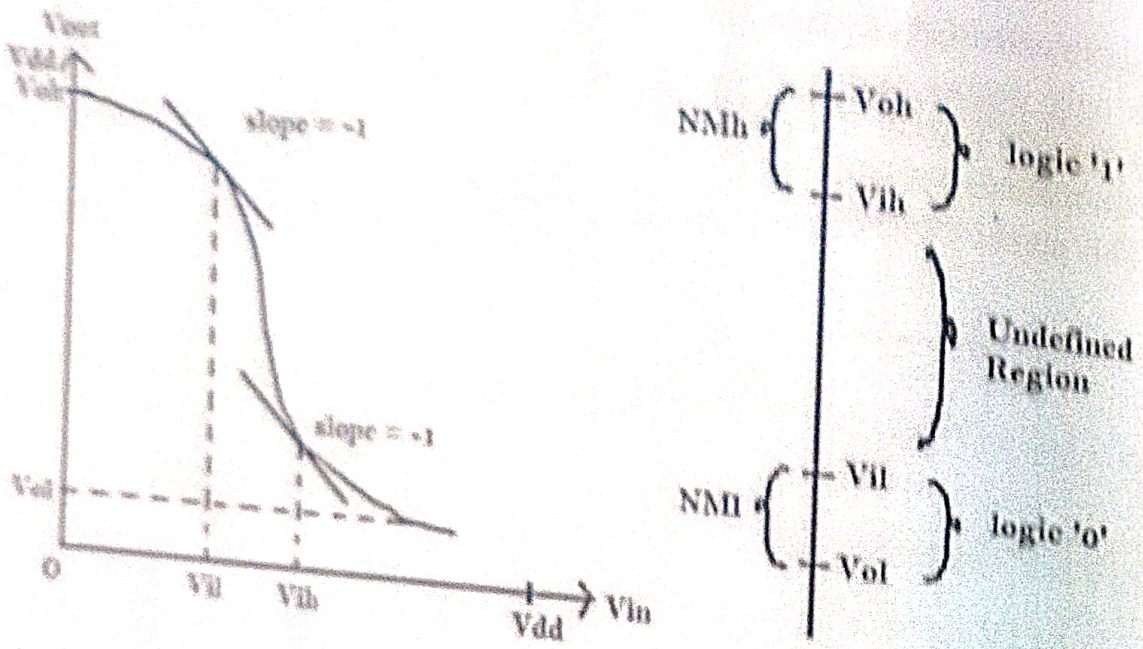


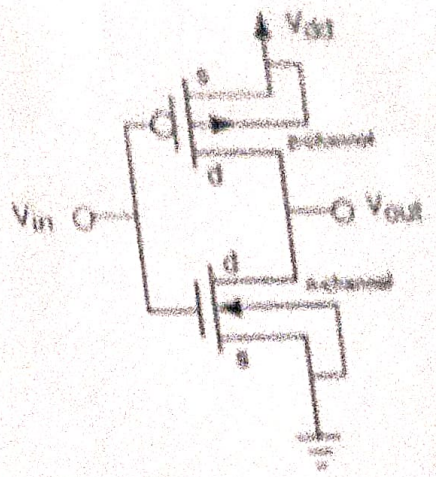
Figure. 3 VTC curve and Noise Margin for CMOS inverter

VIH and VIL are the operational points of the inverter where $\frac{dV_{out}}{dV_{in}} = -1$. In the terminology of the analog circuit designer, these are the points where the gain g of the amplifier, formed by the inverter, is equal to - 1. A simpler approach is to use a piecewise linear approximation for the VTC, as shown in Figure 3. The transition region is approximated by a straight line, the gain of which equals the gain g at the switching threshold VM. The crossover with the VOH and the VOL lines is used to define VIH and VIL points. Nosie margin is given by

NM_L (NOISE MARGIN low) = VIL – VOL

NM_H (NOISE MARGIN high) = VOH – VIH

Circuit diagram:



Procedure:

1. Draw the circuit in LT spice as per circuit diagram
2. Plot voltage transfer curve by varying input voltage Vin from 0v to 3.3V
3. Plot transfer curve for different values of R and observe voltage transfer curve.
4. Plot output waveform of inverter by giving Square input of 1 KHz and 3.3V
5. Calculate noise margin from the graph

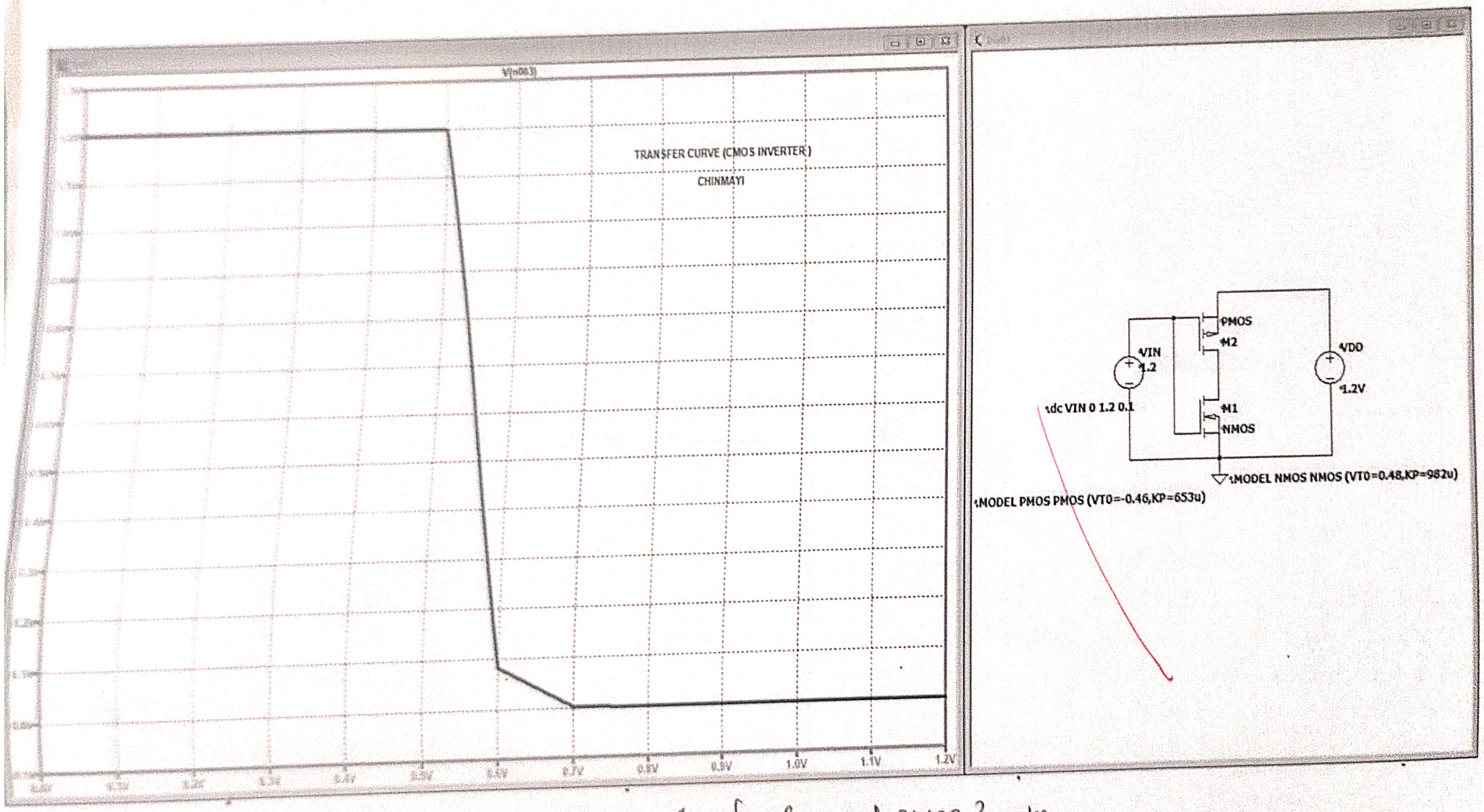


Figure 4. Transfer Curve of CMOS Inverter

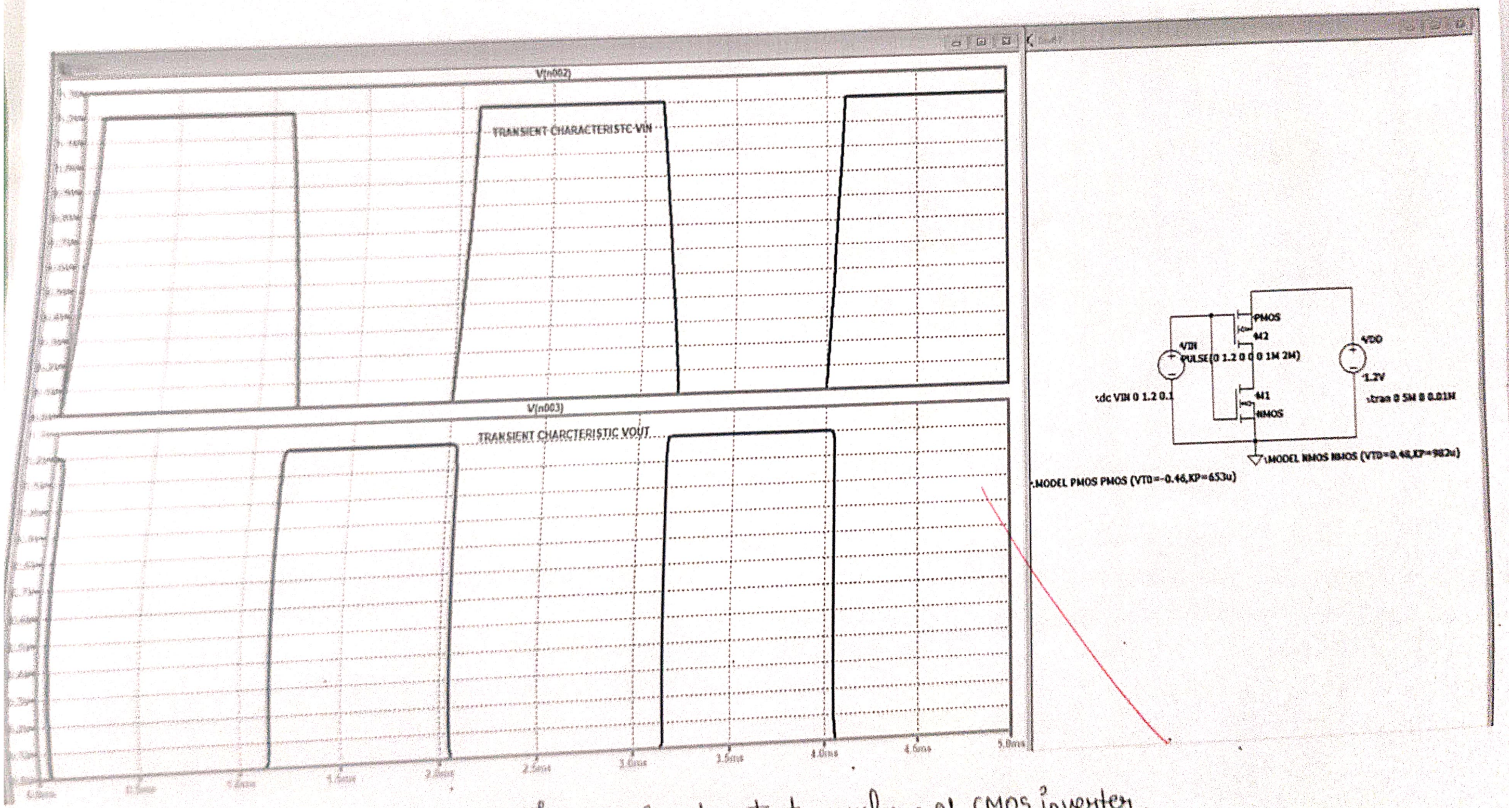


Figure 5. Input output waveform of CMOS inverter

Calculation &

$V_{DD} = 1.2V$ · $V_{TN} \neq V_{TP}$

$V_{TN} = 0.48V$

$V_{TP} = -0.46V$

$k_n = 982 \mu A/V^2$

$k_p = 653 \mu A/V^2$

$$V_{IH} = \frac{2V_O + V_{TP} - V_{DD} + k_R \cdot V_{in}}{1 + k_R}$$

$$V_{IL} = \frac{2V_O - 0.938}{2.503}$$

$$V_{IL} = 0.799V_O - 0.379$$

$$\frac{K_D}{2}(V_{GSn} - V_{TD})^2 = \frac{k_p}{2}\left[2(V_{GSP} - V_{TP})V_{DSP} - V_{DSP}^2\right]$$

$$k_R (V_{GSn} - V_{Tn})^2 = \left[2(V_{GSP} - V_{TP})V_{DSP} - V_{DSP}^2\right]$$

$$1.503((0.799V_O - 0.379) - 0.48)^2 = \left[2(0.799V_O - 0.379 - 1.2 + 0.46)(V_O - 1.2V) - (V_O - 1.2)^2\right]$$

$$0.362V_O^2 - 0.306V_O - 0.137 = 0$$

$V_O = 1.169$

$V_O = -0.323$

V_O cannot be negative

hence $V_O = 1.169$

$\therefore \boxed{V_{IL} = 0.55V}$

$$V_{IH} = \frac{V_{DD} + V_{TP} + k_R(2V_O + V_{Tn})}{1 + k_R}$$

$$V_{IH} = \frac{1.2 + (-0.46) + 1.503(2V_O + 0.48)}{1 + 1.503}$$

$$V_{IH} = 0.58 + 1.2V_O$$

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$$K_R\left[2(V_{GMSN}-V_{TN})V_{DSN}-V_{DSn}^2\right)=(V_{GMSR}-V_{TP})^2$$

$$1.503\left[2(0.58+1.2V_o-V_m)V_o-V_o^2\right)=(0.58+1.2V_o-V_{DD}-V_{TP})^2$$

$$0.665V_o^2+0.687V_o-0.024=0$$

$$V_o=-1.068V$$

$$V_o=0.034V$$

$$V_{IH}=0.58+1.2V_o$$

$$\boxed{V_{IH}=0.623V}$$

$$NM_L=V_{IL}-V_{OL}=0.55-0=0.55V$$

$$\boxed{NM_L=0.55V}$$

$$NM_H=V_{OH}-V_{IH}=1.2-0.623$$

$$\boxed{NM_H=0.577V.}$$

Result Table:-

Sr.no	Parameters	Theoretical	from graph
1	V_{IL}	0.55V	0.50V
2	V_{IH}	0.623V	0.60V
3	V_{OL}	0V	0V
4	V_{OH}	1.2V	1.2V
5	NM_H	0.577V	0.6V.
6	NM_L	0.55V	0.5V

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Result analysis and Conclusion

The transient and transfer characteristics of a CMOS inverter reveal its switching behaviour and voltage transfer properties. By plotting these characteristics, we can analyse key parameters such as propagation delay, noise margins and threshold voltage, which are crucial for threshold voltage, which are crucial for determining the inverters performance, speed and stability. In digital circuits, ensuring reliable logic level transitions in CMOS based system.

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Post Experiment questions:

Q1.] How to form symmetrical CMOS inverter?

→ To form a Symmetrical CMOS inverter, where the Pull up (PMOS) and pull down (NMOS) networks have similar characteristics follow these steps:

① OR (+) → parallel connected drivers

② AND (X) → Series Connected drivers

③ The pull up and pulldown networks are dual of each other.

To form a Symmetrical CMOS inverter, match the threshold Voltage (V_{TH}) of the NMOS and PMOS transistors. Adjust their width to length ratios, typically making the NMOS to balance current drive strength due to mobility differences. Minimize parasitic capacitance and carefully design the layout to ensure balance rise and fall times, creating a symmetrical Inverter with stable and optimized switching characteristics of digital circuits.

Q2) Power consumption of CMOS inverter is less than Resistive load Inverter, Justify.

→ The lower power consuption of a CMOS inverter is primarily due its almost zero static power consumption & low dynamic power consumption. This makes CMOS technology highly efficient for digital circuits especially in battery-operated and low power applications.

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Name of Student:	Chinmayi Umesh Upadhya
Roll No. :	48
Practical No.:	07
Title of Practical:	To realize NAND & NOR Gate & verify truth table in LTspice.
Date of Submission:	
Date of Correction:	

Evaluation

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Performance	5	05
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Journal work and timely submission	8-10	6-7	2-3

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Name of Faculty: S. Ichaun

Signature:

Date: 12/9/24

Experiment No. 07

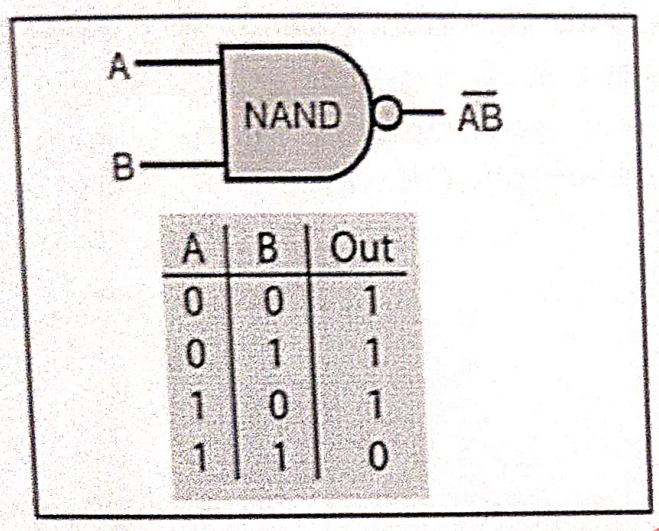
Aim : To realize NAND and NOR gates and verify truth table in LTspice software.

Software: _LTspice software.

Theory:

▯ NAND Gate

The logic or Boolean expression given for a logic NAND gate is that for *Logical Addition*, which is the opposite to the AND gate, and which it performs on the *complements* of the inputs. The Boolean expression for a logic NAND gate is denoted by a single dot or full stop symbol, (.) with a line or *Overline*, (¯) over the expression to signify the NOT or logical negation of the NAND gate.



A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

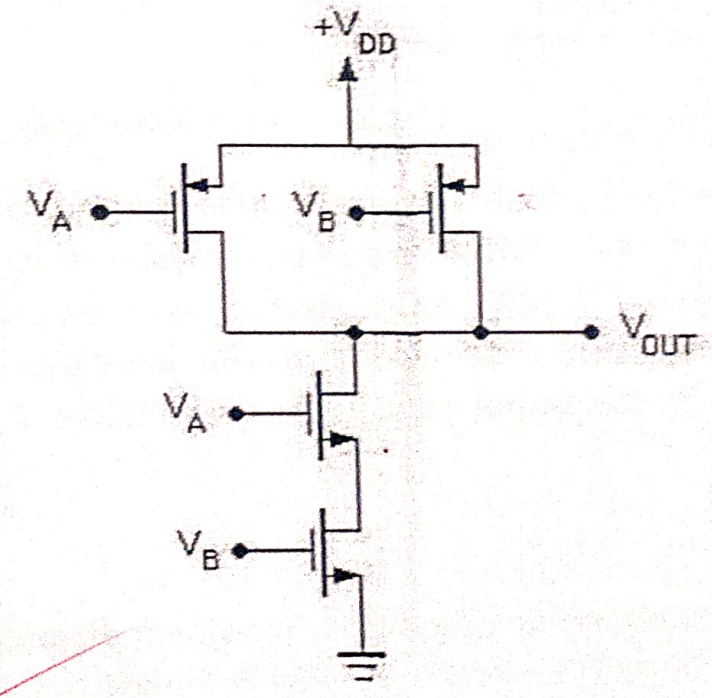


Figure.1 NAND Gate using CMOS logic

CMOS implementation of a two-input NAND gate consist of pull-down sub-circuit made of a series combination of two NMOS transistors as shown in figure1. These are responsible for conducting logic '0' to the output node when both of the gates are at logic '1'. The pull-up path on the other hand consists of a parallel combination of two PMOS transistors. If either of the logic is `0', the output node assumes the value `1'.

▯ NOR Gate:

The logic or Boolean expression given for a logic NOR gate is that for *Logical Multiplication* which it performs on the *complements* of the inputs. The Boolean expression for a logic NOR gate is denoted by a plus sign, (+) with a line or *Overline*, (¯) over the expression to signify the NOT or logical negation of the NOR gate.

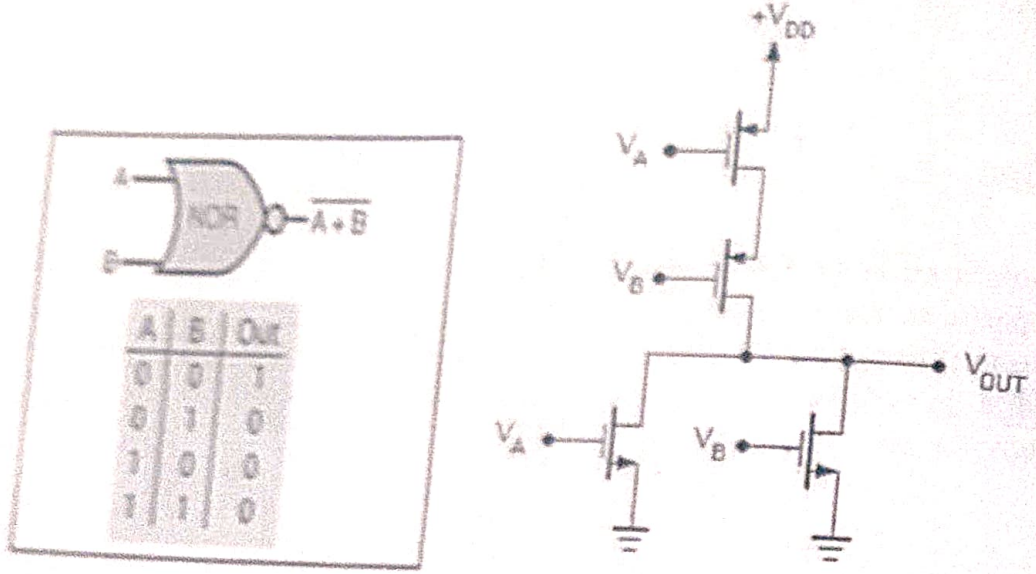


Figure.2 NOR Gate using CMOS logic

implementation of a two-input NOR gate consists of pull-up sub-circuit made of a series combination of two PMOS transistors as shown in figure 2. These are responsible for conducting logic '1' to the output node when both of the gates are at logic `0'. The pull-down path on the other hand consists of a parallel combination of two NMOS transistors. If either of the logic is '1', the output node assumes the value '0'.

Procedure:

1. Draw the circuit in LT spice as per circuit diagram.
2. Apply appropriate supply voltage and Input signal.
3. Simulate the circuit and Check the functionality of circuit.
4. Verify truth table.

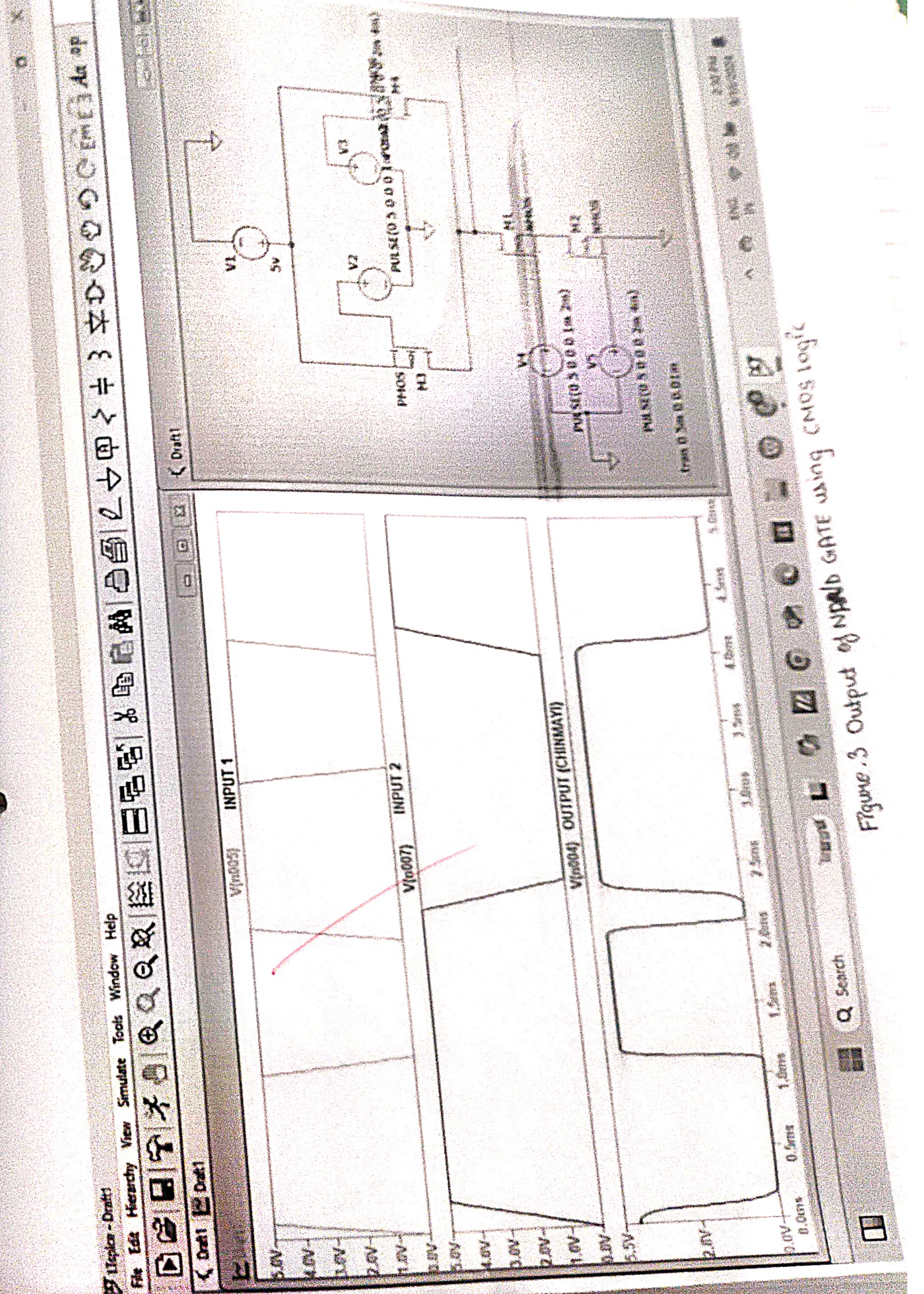


Figure.3 Output of NAND GATE using CMOS logic

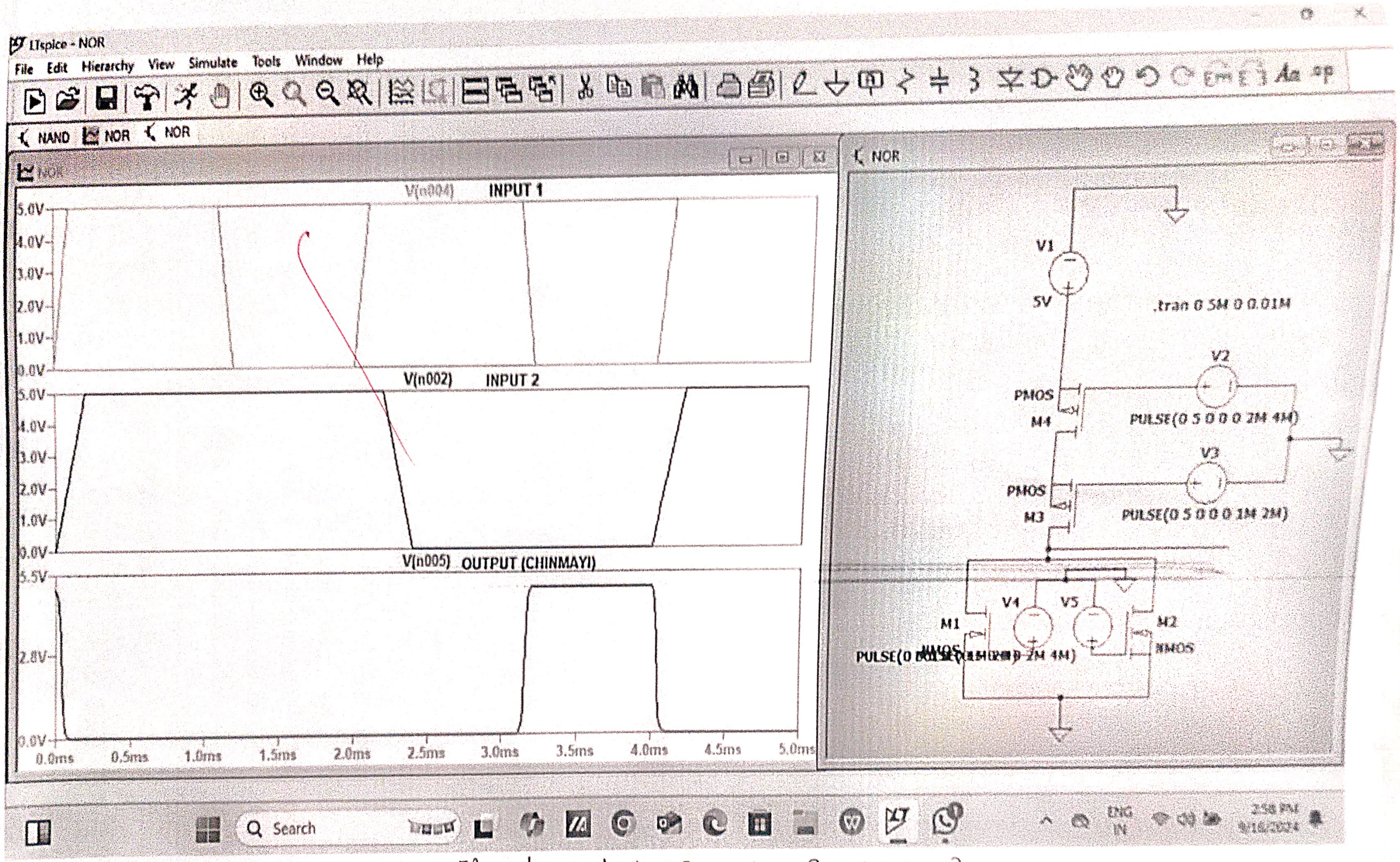


Figure 4 Output of NORD Gate using CMOS logic

Result analysis and Conclusion:

In this experiment we have realize NAND & NOR gate using CMOS inverter logic. As CMOS acts as inverter So to realize NAND we have to make a CMOS with respect to AND & for NOR we have to make a CMOS with respect to OR. For 'AND' we put nmos in series and pmos in ~~parallel~~ Parallel & for 'OR' we put nmos in parallel and pmos in series. By arranging pmos & nmos we get y (output) which will Inverte the AND and OR gate output making it NAND and NOR respectively.

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Post Experiment Questions

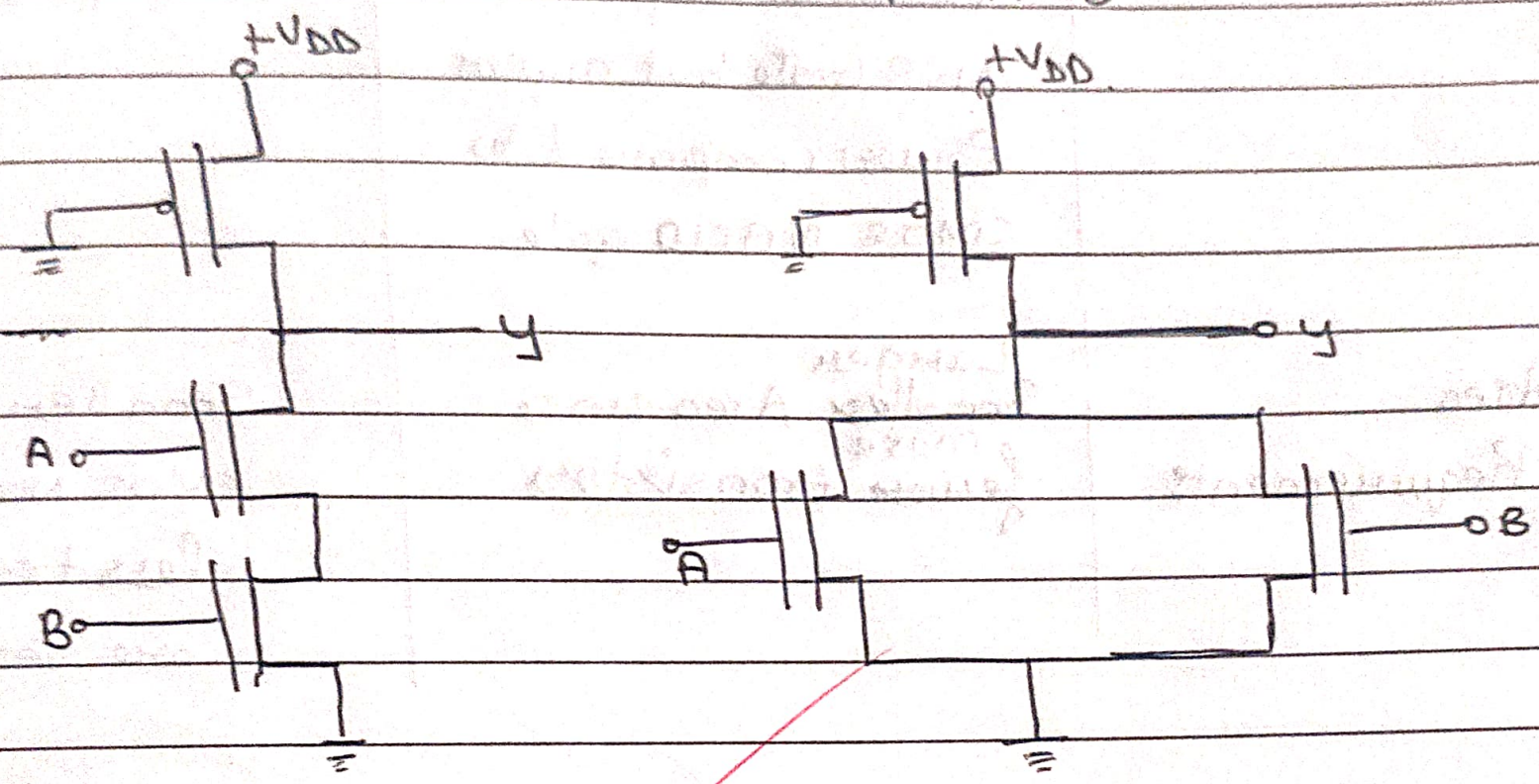
01] Realize NAND & NOR using pseudo logic.

→ NAND using pseudo logic

$Y = \overline{A.B}$

NOR using pseudo logic

$Y = \overline{A+B}$



NAND NOR

02] Compare NAND and NOR realization using CMOS and pseudo logic based on power and area requirements.

→ Parameter	CMOS NAND Gate	Pseudo-logic NAND Gate
Power Consumption	Low Power consumption due to low static current in steady states	Moderate Power, slightly higher than CMOS - Power savings depend on load capacitance & operating conditions.
Area Requirements	~~Smaller~~ Larger Area since ~~fewer~~ more transistors are required. - Typically requires 4 transistors	Smaller Area since fewer transistors are required. Typically requires 3 transistors

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Parameter	CMOS NOR Gate	Pseudo-logic NOR Gate
Power Consumption	Lower Power Compared to Pseudo-logic NOR Gate but higher Power compared to CMOS NAND gate.	Higher Power Compared to CMOS NOR Gate due to capacitive load.
Area Requirements	Larger ~~Smaller~~ Area since more ~~fewer~~ transistors	Smaller Area than CMOS NOR gate since less transistors are required.

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Signature:

Date:

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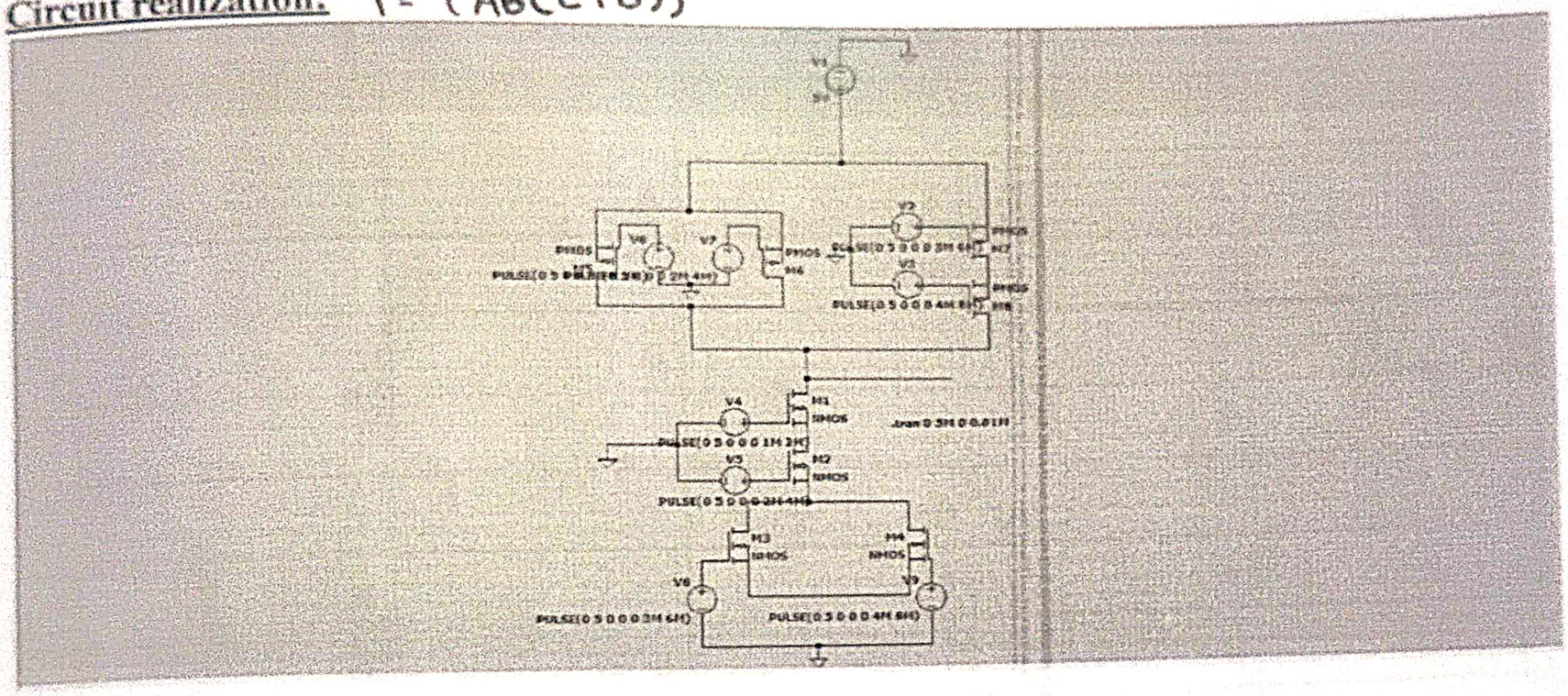
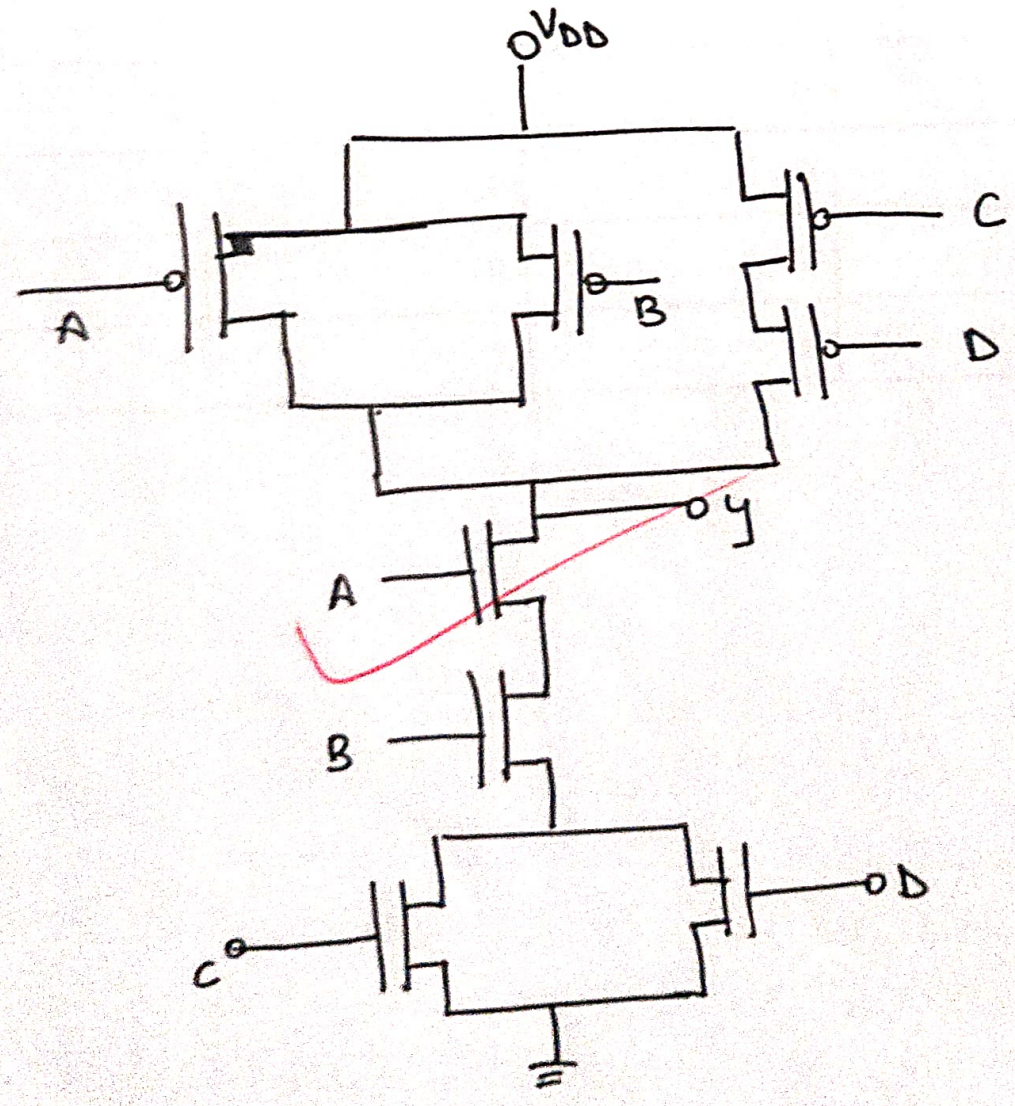
Experiment No: 8

Aim: Realize any expression using any logic style and verify its operation using LT spice.

Software: LT Spice.

Circuit realization: $Y = \overline{(AB(C+D))}'$





Truth Table:

A	B	C	D	Y=(AB(C + D))'
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

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Procedure:

1. Draw the circuit in LT spice as per circuit diagram.
2. Apply appropriate supply voltage and Input signal.
3. Simulate the circuit and Check the functionality of circuit.
4. Verify truth table.

Output :

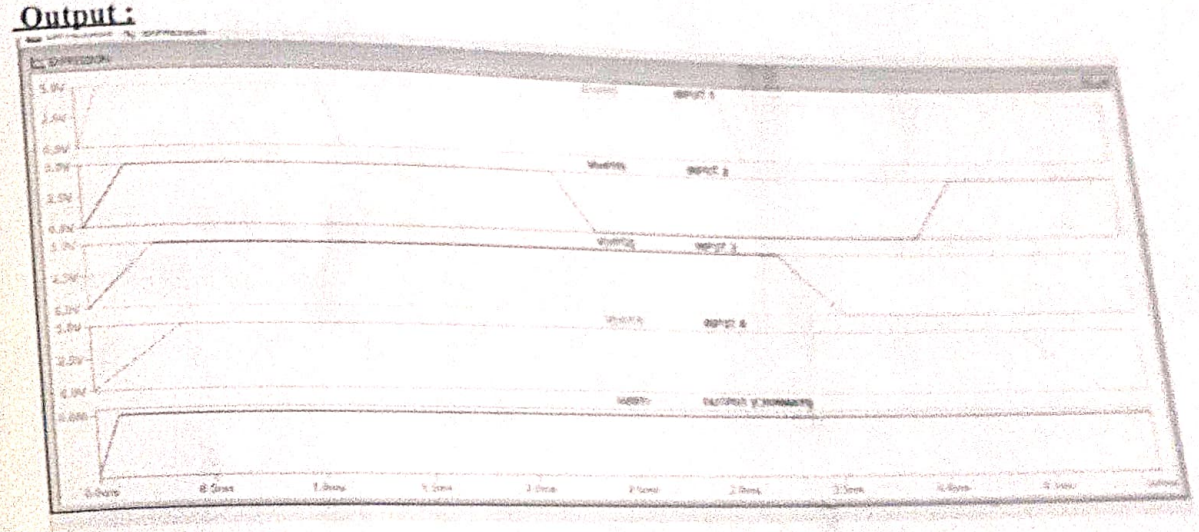

Figure .1 Output of Expression realization

Result and Conclusion:

$$Y=\overline{(AB(C+D))}$$

The given expression has been successfully realized using CMOS logic in LTspice. The simultation results accurately reflect the expected truth table behaviour demonstrating the correct functionality of the circuit. The output waveform matches the expected truth table values, exhibits proper timing characteristics, etc. confirms the successful operation of the realized expression. This outcome validates the effectiveness of the choosen logic style & the accuracy of the circuit implementation.

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Signature:

Date: 24/9/24

Experiment No. 09

Aim: To realize 2:1 mux using Pass transistor logic in LT spice software.

Software: _LT spice software.

Theory: A multiplexer is a device that combines several analog or digital input signals and forwards them into a single output line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send at the output. For 2:1 MUX, there are two input lines, and one select line.

2:1 MUX using Pass Transistor Logic:

To realize 2:1 mux using pass transistors logic, a greater number of transistors are required as compared to pass transistor logic. Pass transistor reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Figure. 1 shows 2:1 MUX using pass transistor logic. When the control signal S is high the lower transistor is ON, and it passes B at the output. Similarly, if the control logic S is low the upper transistor is ON, and it passes A at the output.

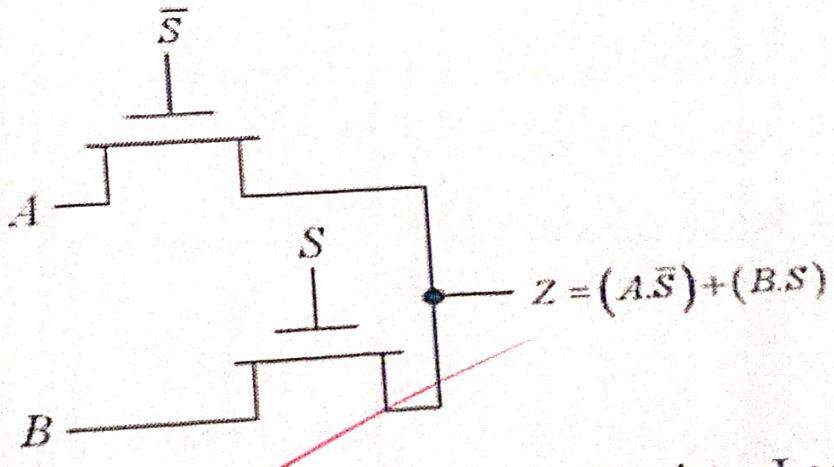
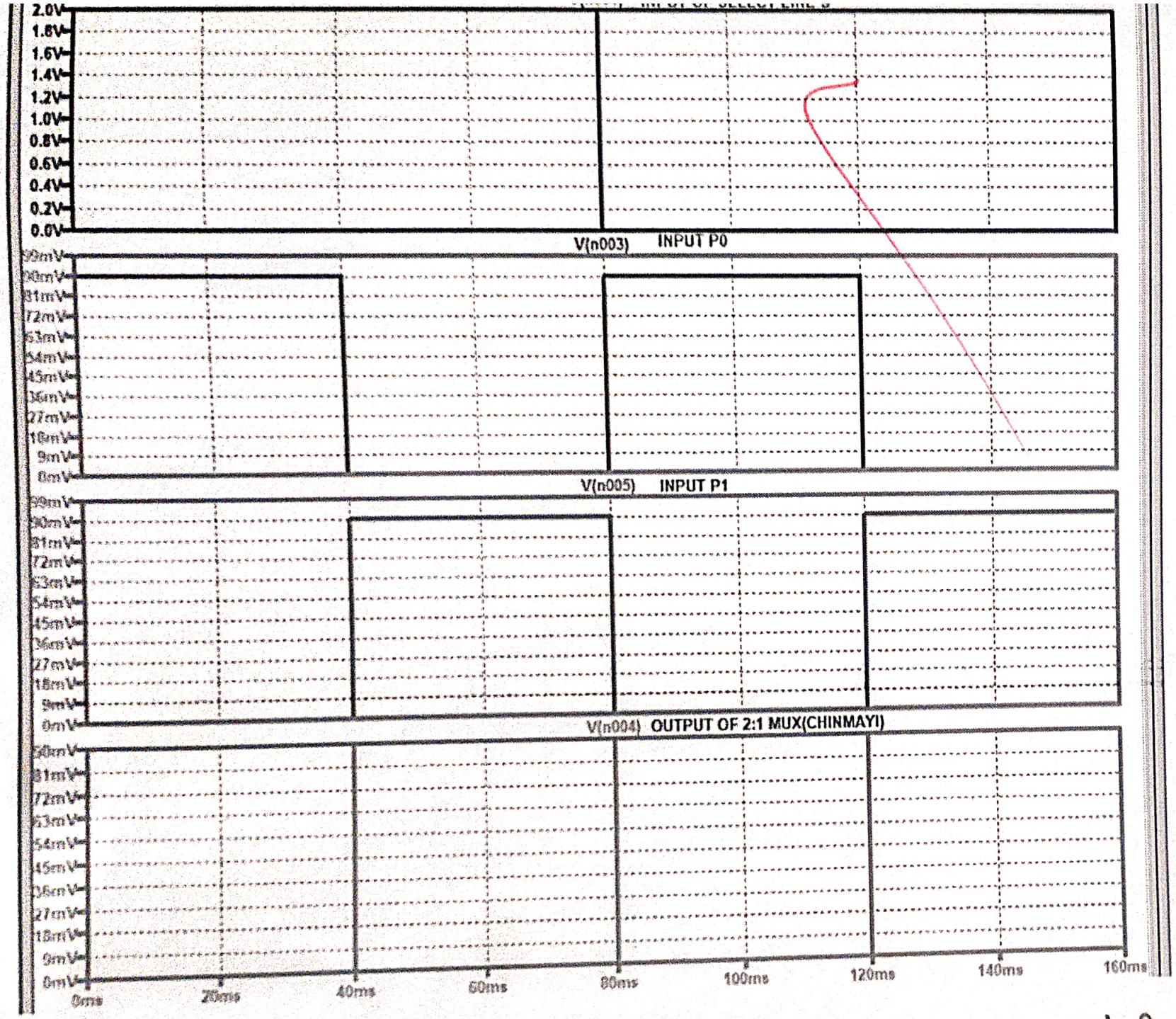


Figure. 1 2:1 MUX using PASS Transistor Logic

Procedure:

1. Draw the circuit in LT spice as per circuit diagram.
2. Apply appropriate supply voltage and Input signal.
3. Simulate the circuit and check the functionality of circuit.



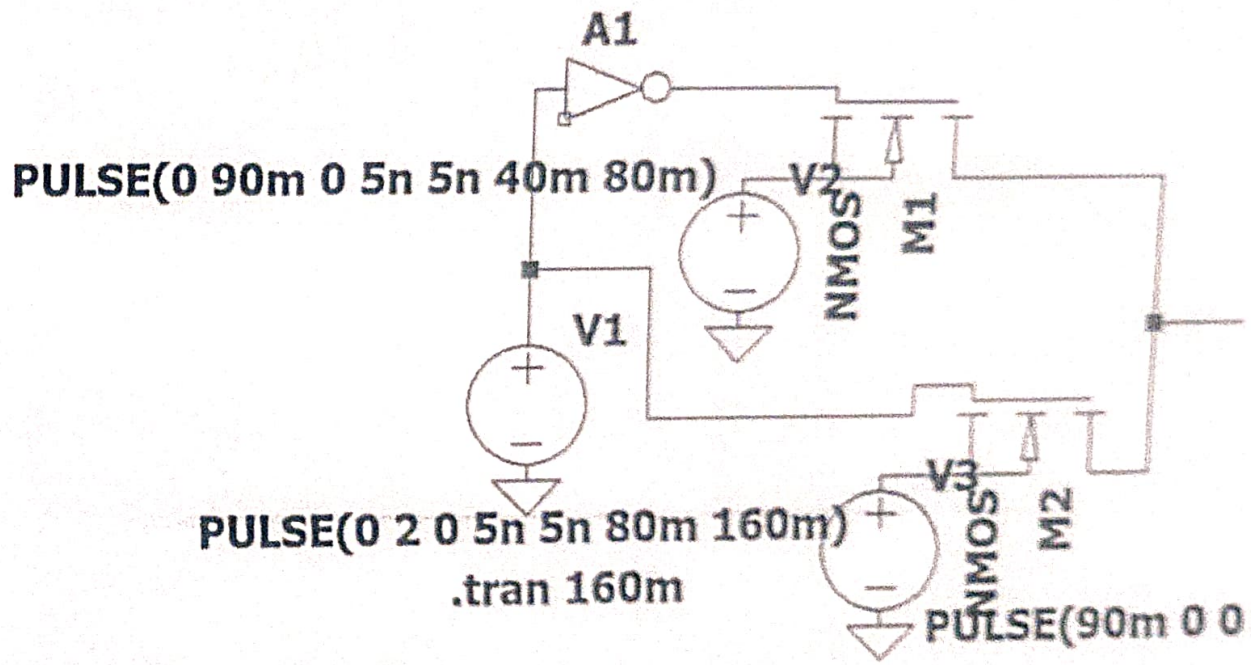


Figure.1. Output of 2:1 MUX using Pass transistor

Result analysis and Conclusion:-

The 2:1 mux Implementation using pass transistor logic, as illustrated in figure 1. output of 2:1 Mux provides a compact & efficient solution for selecting between two input signals. The use of pass transistors allows for a reduction in the number of active devices compared to traditional logic gate realization, leading to a smaller area footprint & potentially lower power consumption. However, the pass transistor approach has a limitation in terms of voltage level degradation, with each stage of the circuit the difference between the high & low logic levels decreases. This can impact the noise margin & overall circuit performance.

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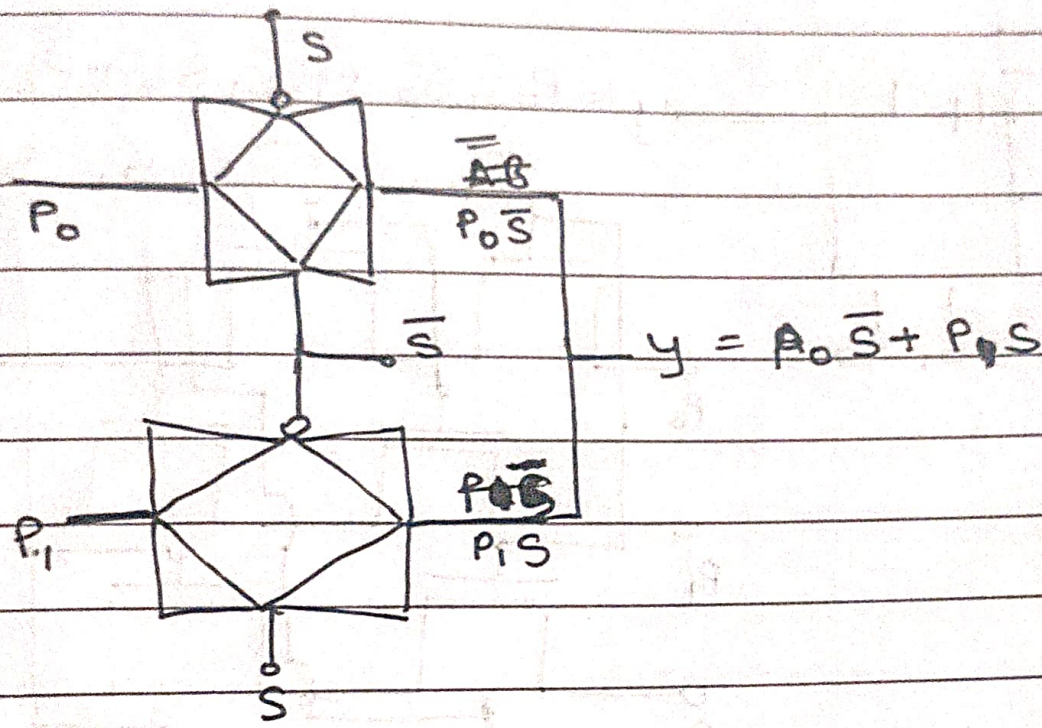
Post experiments Questionse

Q1) Realize 2:1 MUX using transmission gate

→ 2:1 Mux using transmission gate



Q2) Compare 2:1 MUX realization using transmission gate & pseudo logic based on power & area required.

Parameter	2:1 MUX realization using transmission gate	2:1 Mux realization using pseudo logic
1) Power	Typically lower static & dynamic power due to the inherent low leakage of MOSFET's & minimal internal node switching.	Higher static power due to the static load, but potentially lower dynamic power due to reduced voltage swing requirements.
2) Area	Smaller area due to the use of two MOSFET's in series	Larger area due to the presence of static load network.

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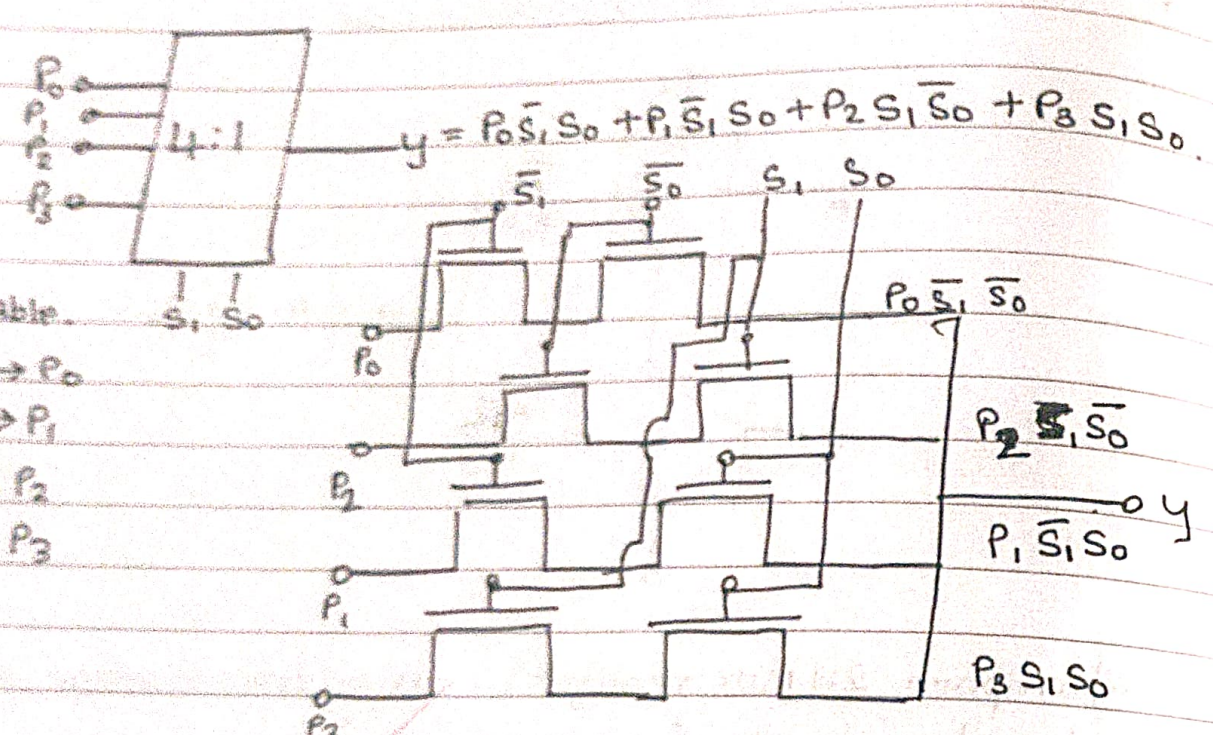
Q5] Realize 4:1 MUX using pass transistor logic

→

4:1 Mux. using pass transistor logic.



Truth table.

S1 S0	
00	→ P0
01	→ P1
10	→ P2
11	→ P3

09/10

9/10/24

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	VLSI

Name of Student:	Chinmayi Umesh Upadhya
Roll No. :	48
Practical No.:	10
Title of Practical:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	04
Journal work and timely submission	10	09
Total	20	18

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

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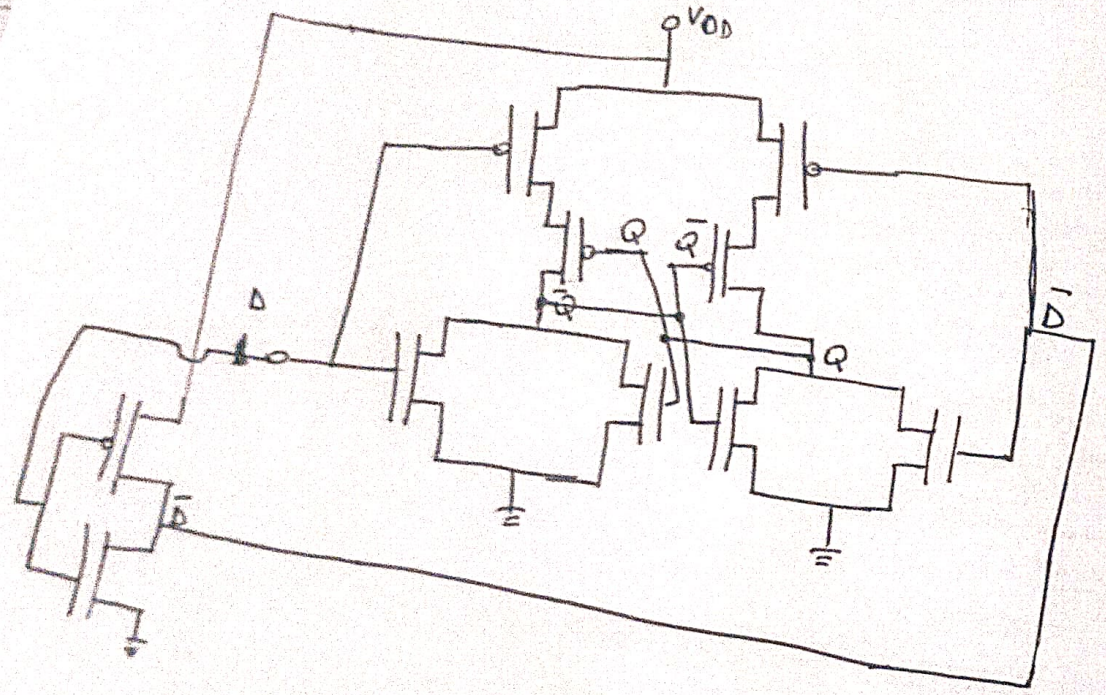

Figure2. CMOS realization of D-latch.

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Experiment No. 10

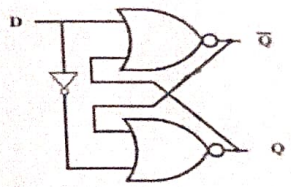
Aim : To implement D-Latch using CMOS logic and verify truth table in LT spice software.

Software: LT spice software.

Theory:

D-Latch:

A D-Latch is a sequential logic circuit that stores one bit of data. It has one input, D, and two outputs, Q and Q'. The D input is the data input, and the Q output is the current state of the latch. The Q' output is the inverse of the current state of the latch.



D	Q	$\bar{Q}$
0	0	1
1	1	0

Figure.1 D-Latch Gate level realization and Truth table

The D-Latch works as follows:

- When the D input is high, the Q output follows the D input.
- When the D input is low, the Q output is latched, and it stores the previous value of the D input.

The D-Latch is a level-sensitive latch, which means that it changes state whenever the D input changes state.

Procedure:

1. Draw the circuit in LT spice as per circuit diagram.
2. Apply appropriate supply voltage and Input signal.
3. Simulate the circuit and check the functionality of circuit.
4. Verify truth table.

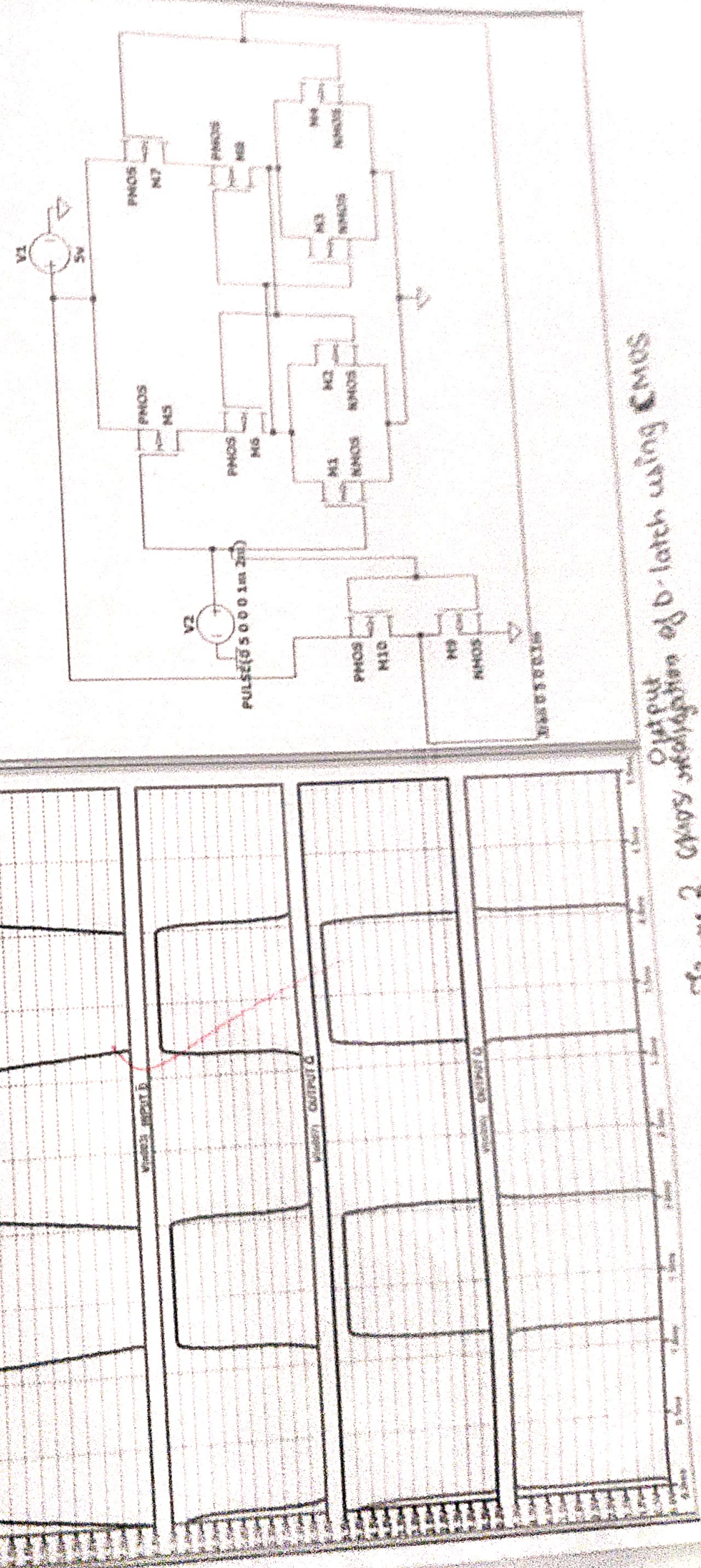


Figure 2 CMOS implementation of D-latch using CMOS

Result analysis and Conclusion

The D-latch, a fundamental building block in digital circuits, has been successfully implemented using CMOS logic. The simulation results in LTspice accurately verified the expected truth table behaviour, demonstrating the device's ability to store & retain one bit of data when the Dinput is high, the Q output follows the Dinput. Conversely when the Dinput is low, the Q output remains latched, preserving the previous value. This level-sensitive characteristic of the D-latch makes it a crucial component in various digital systems, enabling the storage & manipulation of data within the circuit.

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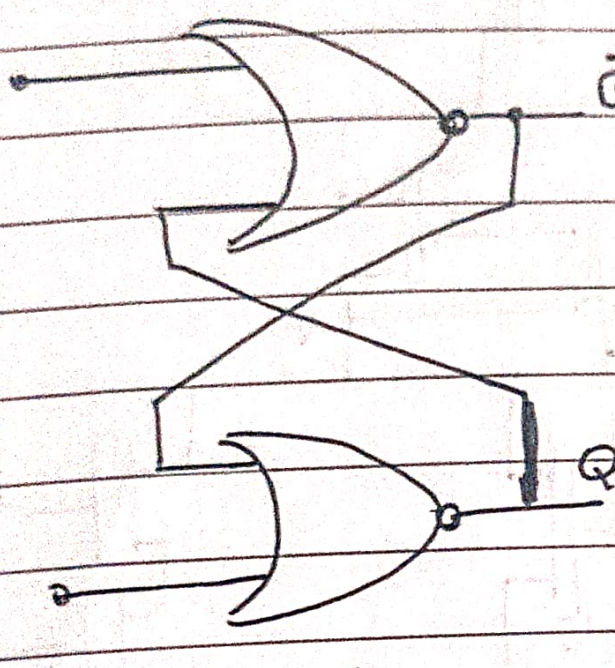
Post Experiment Questions:-

Q1] Realize SR latch using CMOS logic

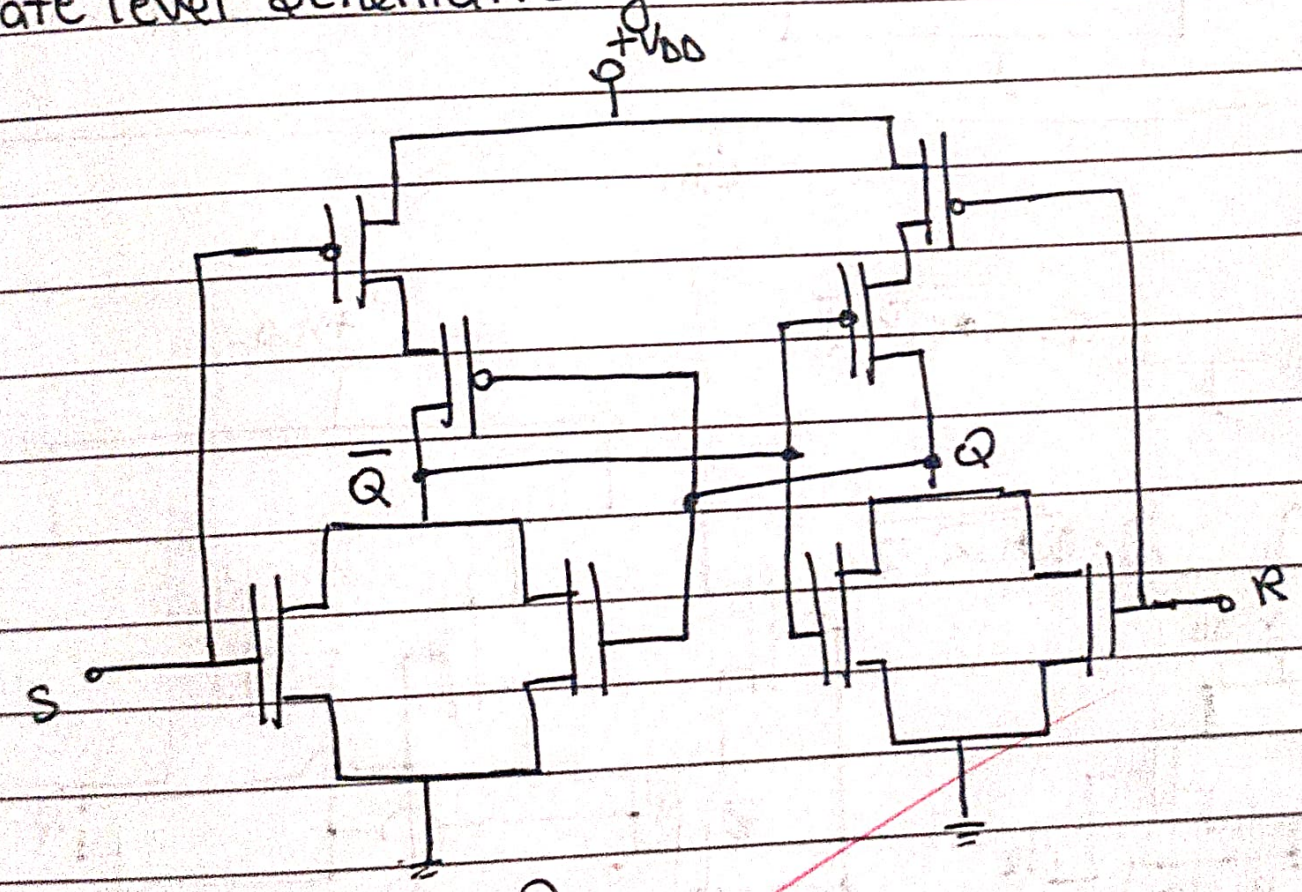
→



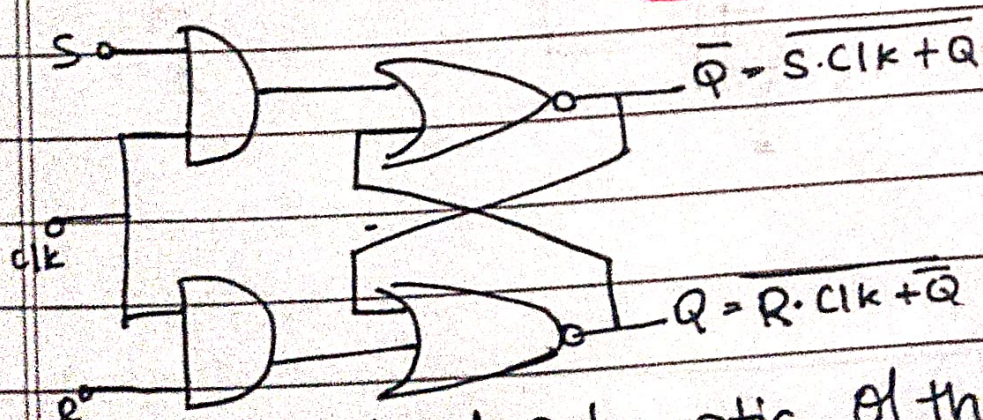
Truth Table

S	R	Q_{n+1}	$\overline{Q}_{n+1}$	Operation
0	0	Q_n	$\overline{Q}_n$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

Gate level Schematic of SR-latch (NOR) based



SR latch (synchronus)



Gate level Schematic of the clock NOR-based SR latch

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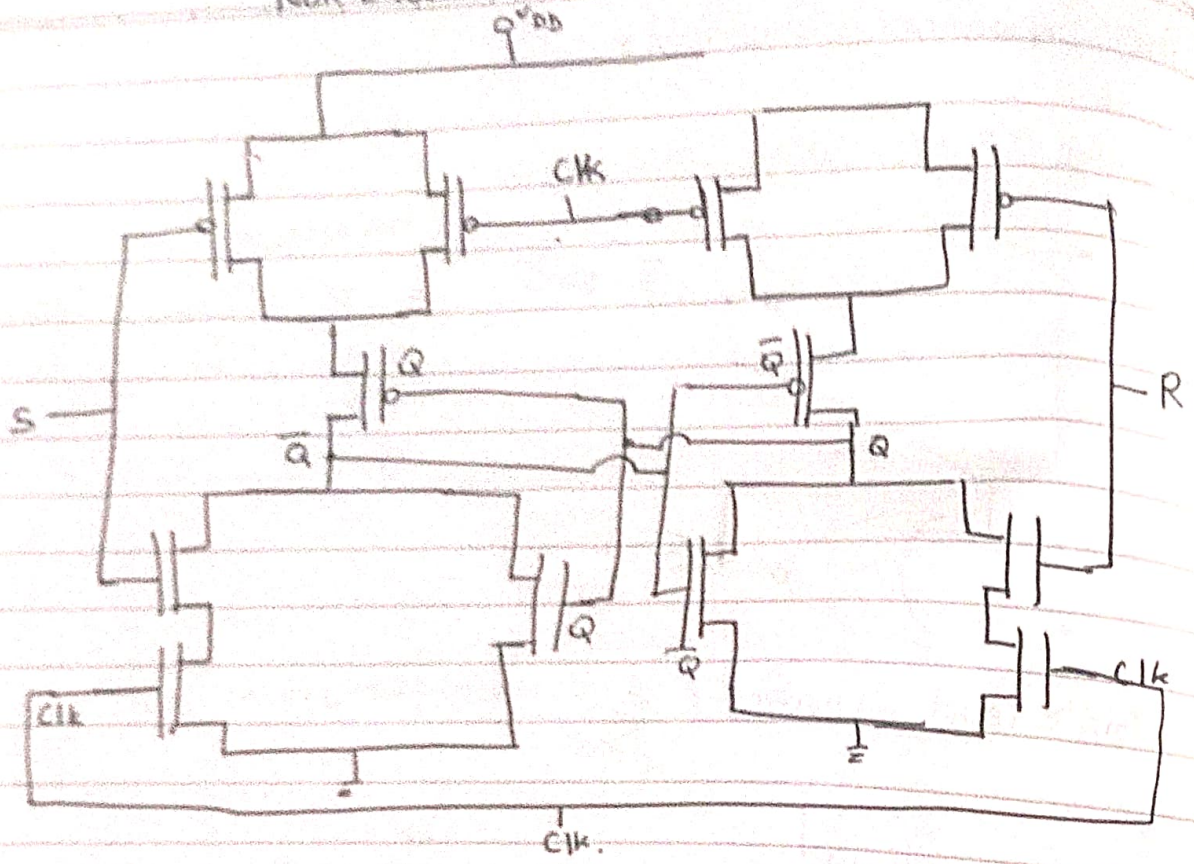
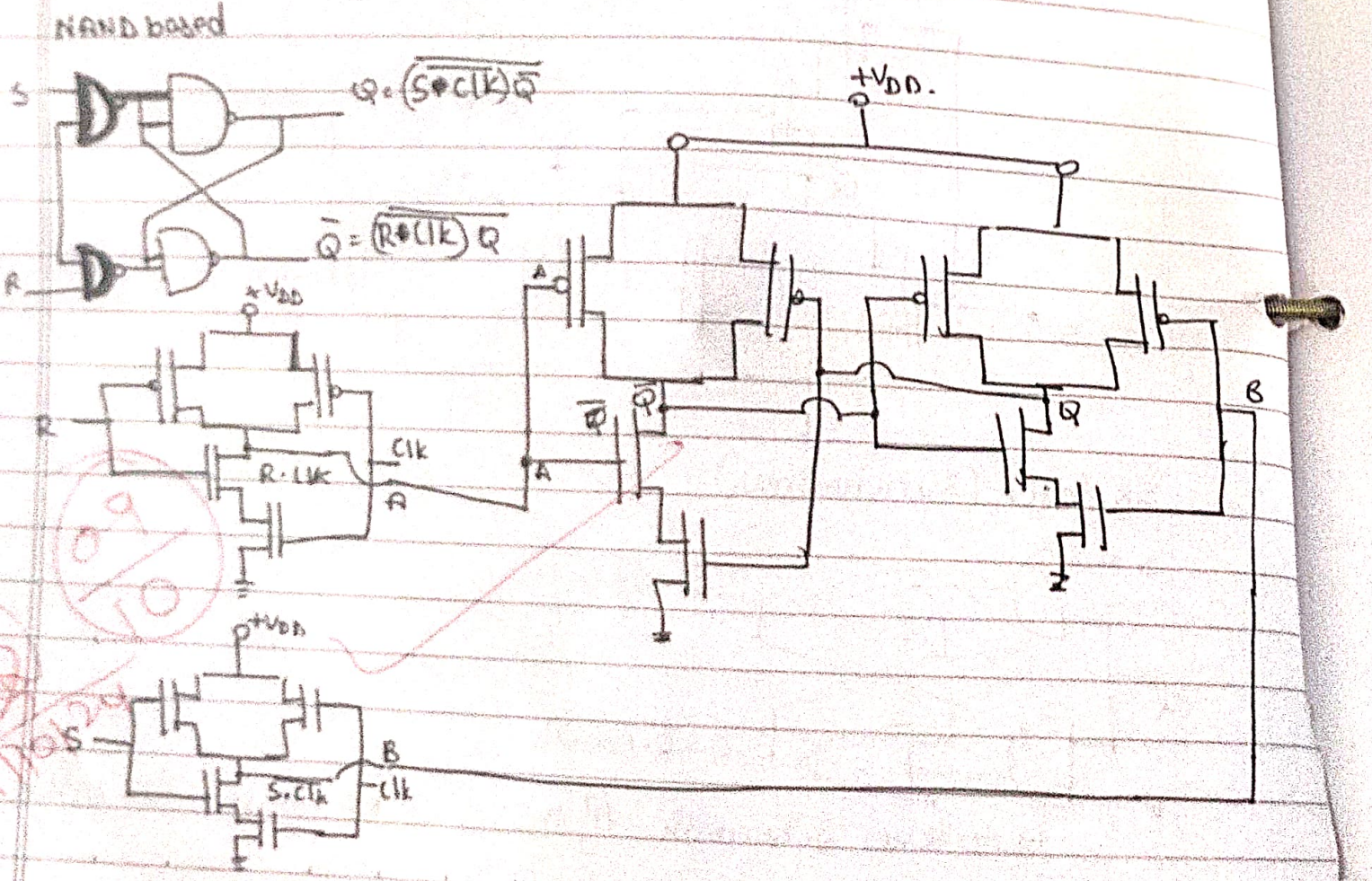
NOR based.



NAND based



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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	I
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmay Umesh Upadhya
Roll No. :	48
Practical No.:	11
Title of Practical:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	05
Journal work and timely submission	10	09
Total	20	18

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
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Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

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Date: 11/10/24

Experiment No: 11

Aim: To Sketch Layout of CMOS Inverter using Microwind.

Software: MICROWIND 3.8

Theory: CMOS is the complementary MOSFET. The p-channel MOSFET relies on an n-type substrate. As commonly p-type wafers are used for processing, an additional n-type well implant is necessary. In this well, which is a deep region of n-type doping, the p-channel MOSFET is placed. As the p-substrate and the n-well junction is reverse biased, no significant current flows between these regions and the two transistors are isolated. The output current of the p-channel MOSFET is typically much lower than the current of an n-channel MOSFET with similar dimensions and dopings. This is due to the lower carrier mobility of holes compared to electrons. As the characteristics of the complementary transistors should be as equal as possible, the width of the p-channel MOSFET is typically made larger to compensate the difference.

Operation:

Figure 1 gives the schematic of the CMOS inverter circuit.

- When Vin is high, Vin ~ Vdd, the voltage between gate and substrate of the nMOS transistor is also approximately Vdd and the transistor is in on-state. The gate-substrate bias at the pMOS on the other side is nearly zero and the transistor is turned off.
- The output voltage Vout is pulled to ground, which is the low state. When the input voltage is in a high-state, the complementary situation occurs and the pMOSFET is turned on while the nMOSFET is turned off.

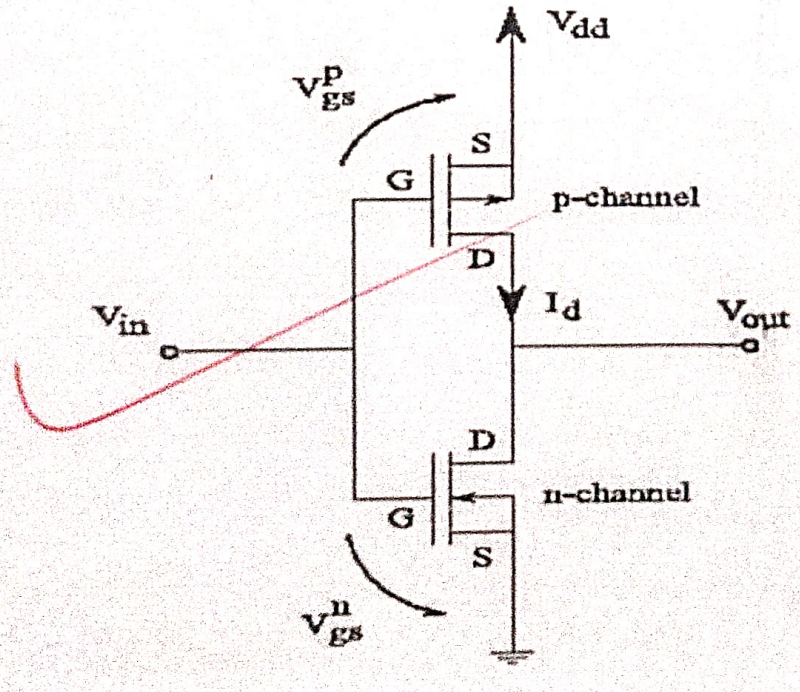


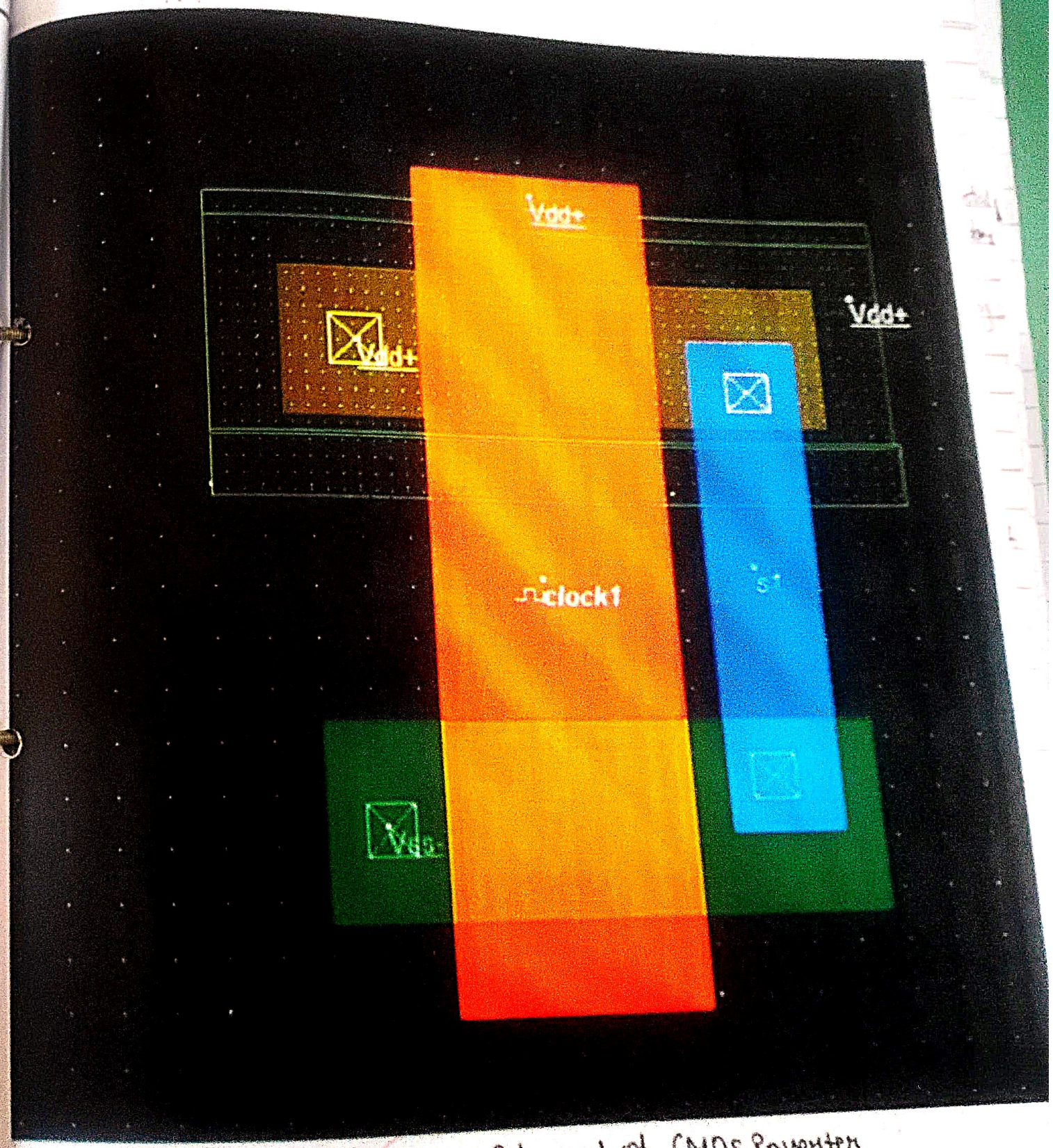
Figure 1. Schematic of a CMOS inverter circuit.

Advantages:

- The outputs actively drive both directions.
- The outputs are rail-to-rail.
- CMOS logic takes very little power when held in a fixed state. The current consumption comes from switching as those capacitors are charged and discharged. Even then, it has good speed to power ratio compared to other logic types.
- CMOS gates are very simple. The basic gate is an inverter, which is only two transistors. This together with the low power consumption means it lends itself well to dense integration. Or conversely, you get a lot of logic for the size, cost and power.

Procedure:

1. Select the foundry.
2. Draw the layout using palette according to lambda based design rules in microwind tool.
3. Apply appropriate supply voltage and Input signal.
4. Connect the visible node to observe output.
5. Check layout with design rule checker for any design rule violation
6. Simulate the circuit from Microwind.
7. Check the functionality of circuit using the truth table.



FPgure 2. layout of CMOS Pnverter

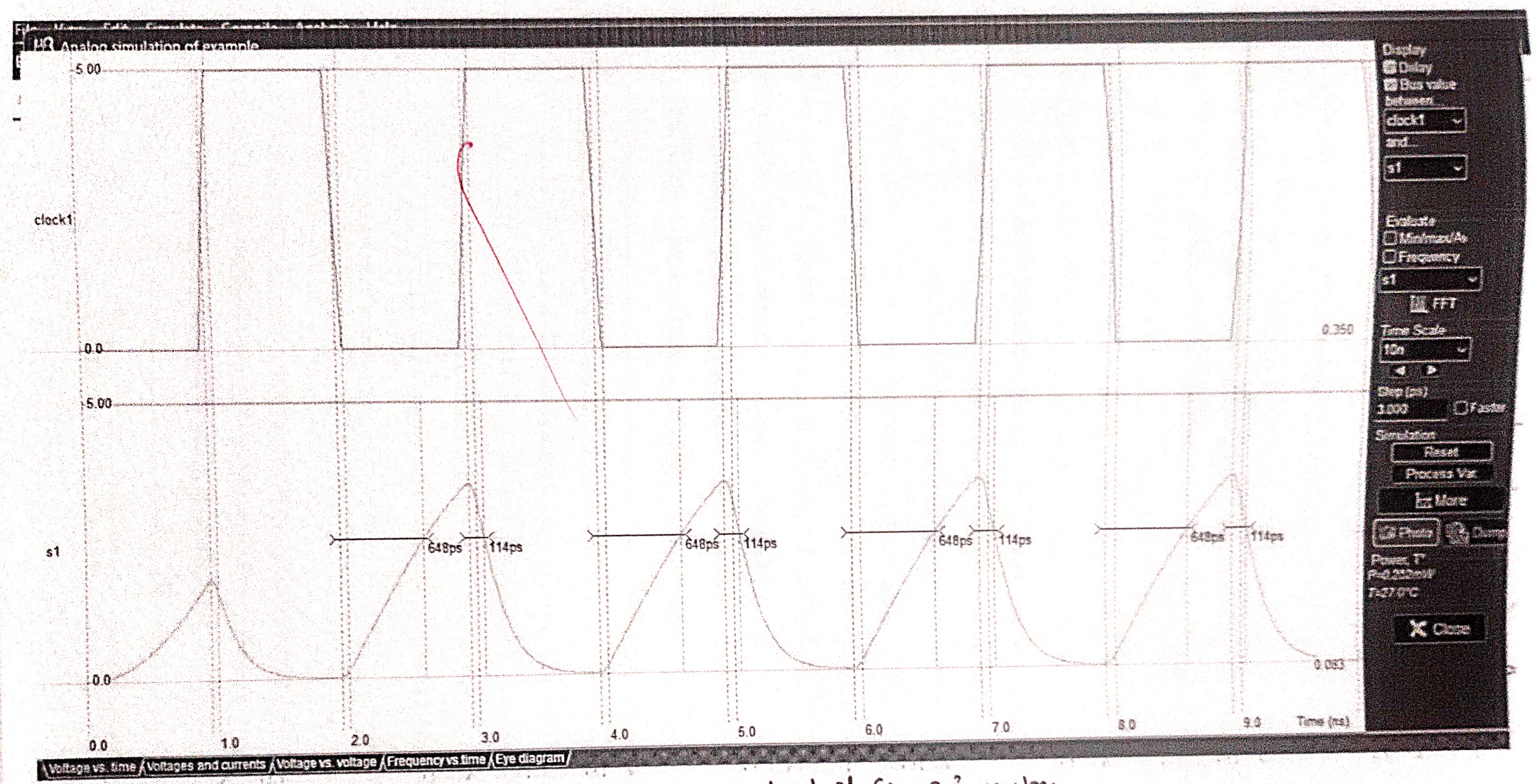
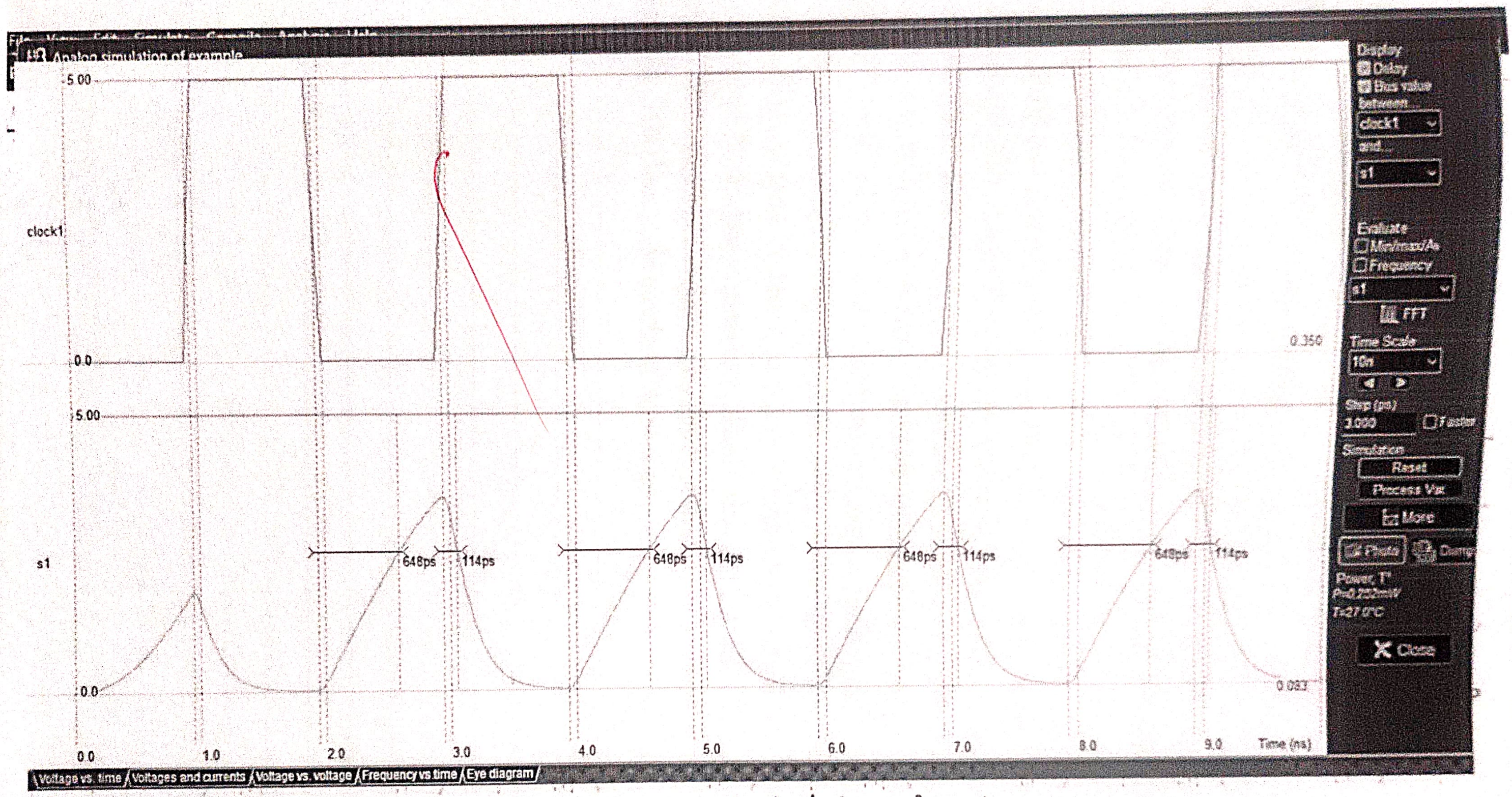


Figure 3. Output of CMOS inverter.



FFgure 3. Output of CMOS inverter.

Result analysis and Conclusion.

In this experiment, we successfully designed and simulated a CMOS inverter layout using Microwind. The Inverter is a fundamental component in CMOS technology, combining nMOS & pMOS transistors. The layout was created following lambda-based design rules to ensure proper functioning & isolation of the transistors. By applying the appropriate input signal and supply voltage, we observed the switching behavior of the inverter, confirming its operation. The simulation results showed the expected output: when the input is high ($V_{in} \approx V_{dd}$), the nMOS is turned on, pulling the output (V_{out}) to ground, while the pMOS is off. Conversely, when the input is low, the pmos turns on, & V_{out} is pulled to V_{dd}. The truth table verified the correct functionality of the CMOS inverter circuit. The design rule checker ensured that the layout adhered to the foundry's rules.

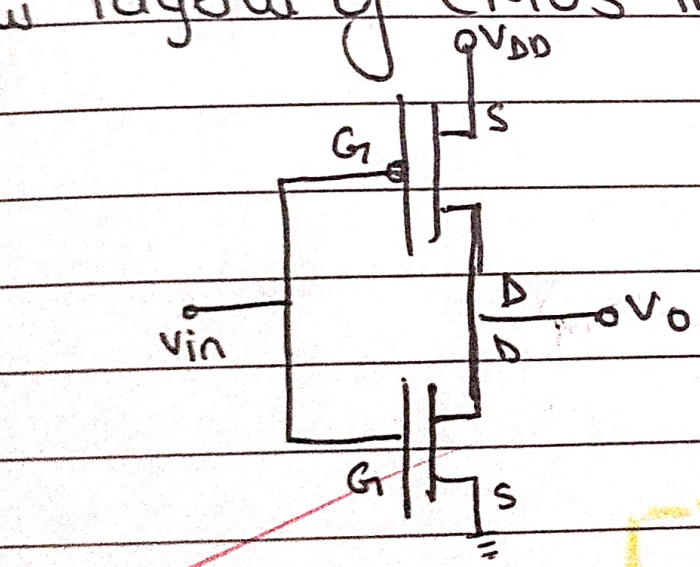
Post Experiment Questions:-

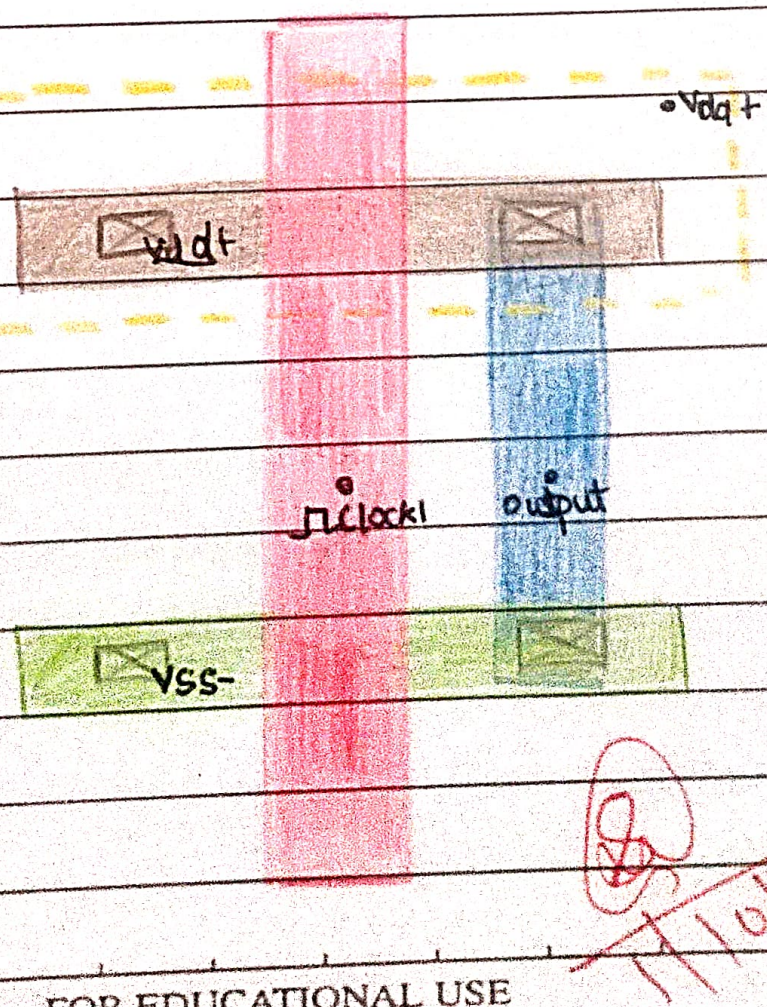
01] Explain lambda based rules

→ lambda based rules are a fundamental aspect of VLSI (very large Scale Integration) layout design, particularly used in tools like Microwind. these rules provide a standardized approach to defining dimensions & spacing in chip design based on a single unit of measurement called "lambda" (λ). In this context, λ is typically half of the minimum feature size of the technology being used.

02] Draw layout of CMOS inverter using lambda-based rule.

→





09/10

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmayi Umesh Upadhya
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Practical No.:	12
Title of Practical:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	4
Journal work and timely submission	10	09
Total	20	18

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

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Name of Faculty:

Signature:

Date: 8/10/24

Experiment No: 12

Aim: To sketch layout of NMOS and PMOS pass transistor switch, transmission gate using microwind.

Software: MICROWIND 3.8

Theory:

Pass Transistor Logic: Pass Transistor Logic Pass Transistor Logic involves nMOS or pMOS transistors to transfer the charge from one node of a circuit to another node under the control of MOS gate voltage. Pass transistor chain can be used in design of regular array based structures such as ROMS PLAs, Multiplexers etc Strength of output signal The strength of a signal is measured by how closely it approximates an ideal voltage source. In general, the stronger a signal, the more current it can source or sink. The power supplies, or rails, (VDD and GND) are the source of the strongest 1s and 0s. nMOS pMOS s Input Output Input Output d Pass transistor strong and degraded outputs An nMOS transistor is an almost perfect switch when passing a 0 and thus we say it passes a strong 0. However, the nMOS transistor is imperfect at passing a 1. The high voltage level is less than VDD so, it passes a degraded or weak 1. A pMOS transistor is an almost perfect switch when passing a 1 and thus we say it passes a strong 1. However, the nMOS transistor is imperfect at passing a 0. The high voltage level is less than VDD, so it passes a degraded or weak 0. AND gate using pass transistor is shown in Figure.1.

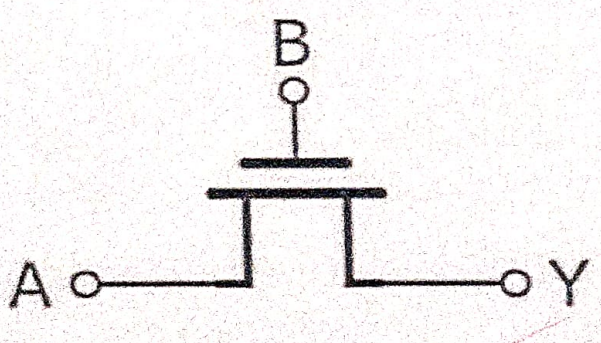


Figure 1. NMOS Pass Transistor as AND gate

Transmission Gate: Connecting PMOS and NMOS devices together in parallel can create a basic bilateral CMOS switch, known commonly as a "Transmission Gate". Transmission gates are quite different from conventional CMOS logic gates as the transmission gate is symmetrical, or bilateral, that is, the input and output are interchangeable. This bilateral operation is shown in figure 2. The transmission gate symbol below which shows two superimposed triangles pointing in opposite directions to indicate the two signal directions.

A transmission gate is a complementary CMOS switch where both the transistors are ON an OFF simultaneously. The NMOS switch passes a good 0 but a poor 1. On the other

hand, the PMOS switch passes a good 1 and a poor 0. Combining them we get a good 0 and a good 1 passed in both the directions.

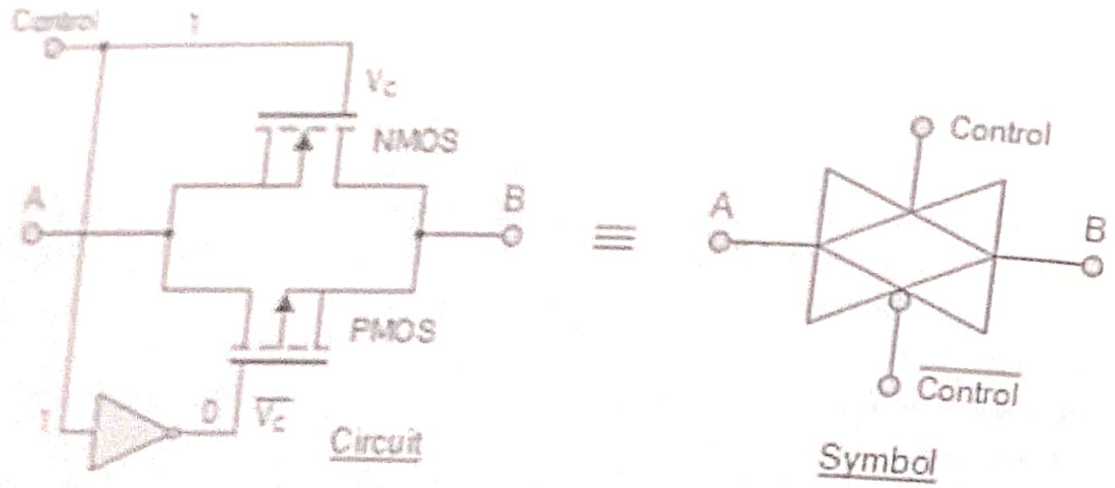


Figure.2 Transmission Gate as AND gate

Procedure:

1. Select the foundry.
2. Draw the layout using palette according to lambda based design rules in microwind tool.
3. Apply appropriate supply voltage and Input signal.
4. Connect the visible node to observe output.
5. Check layout with design rule checker for any design rule violation
6. Simulate the circuit from Microwind tool.
7. Check the functionality of circuit and voltage levels.

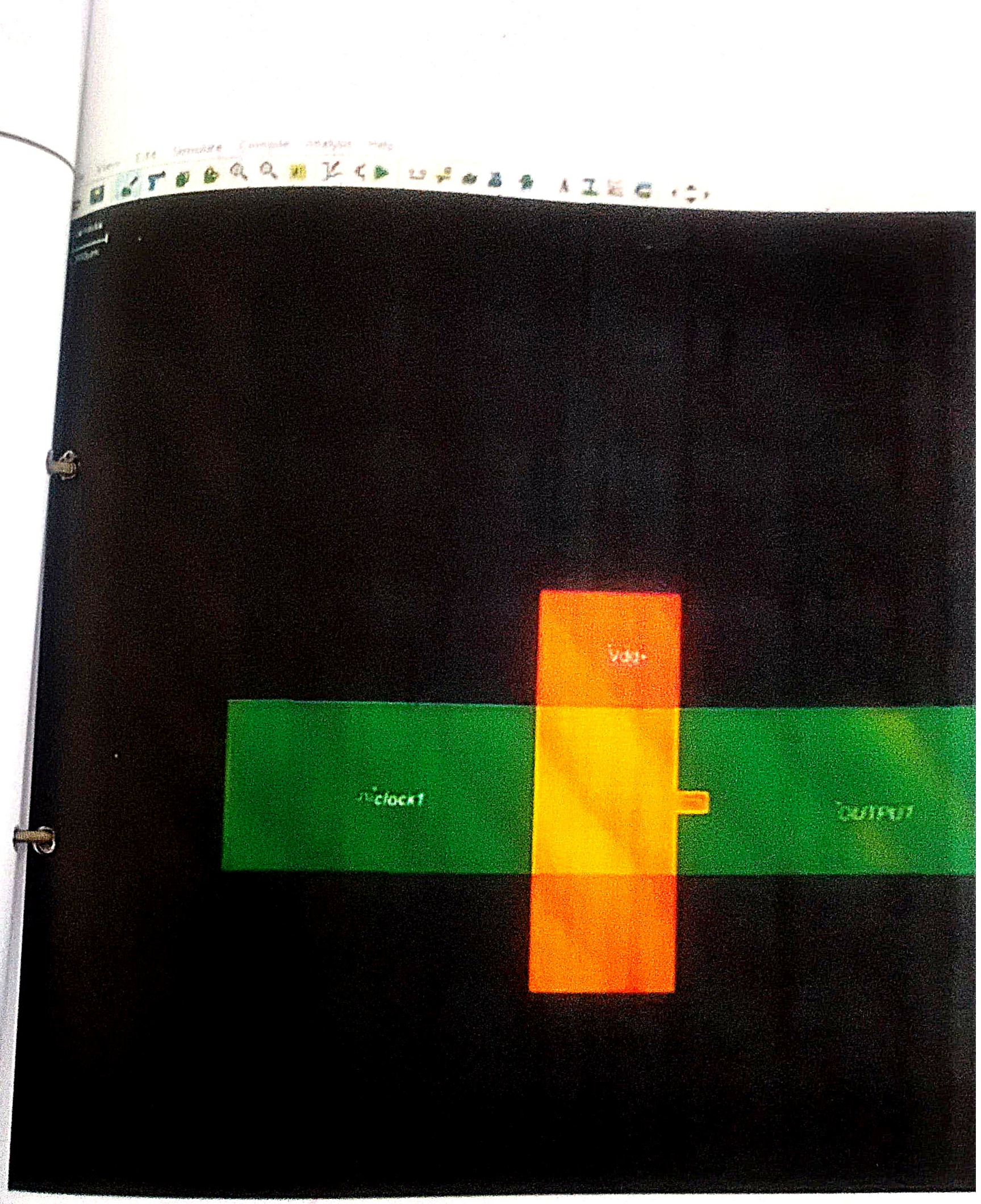


Figure 3.1 layout of NMOS pass transistor

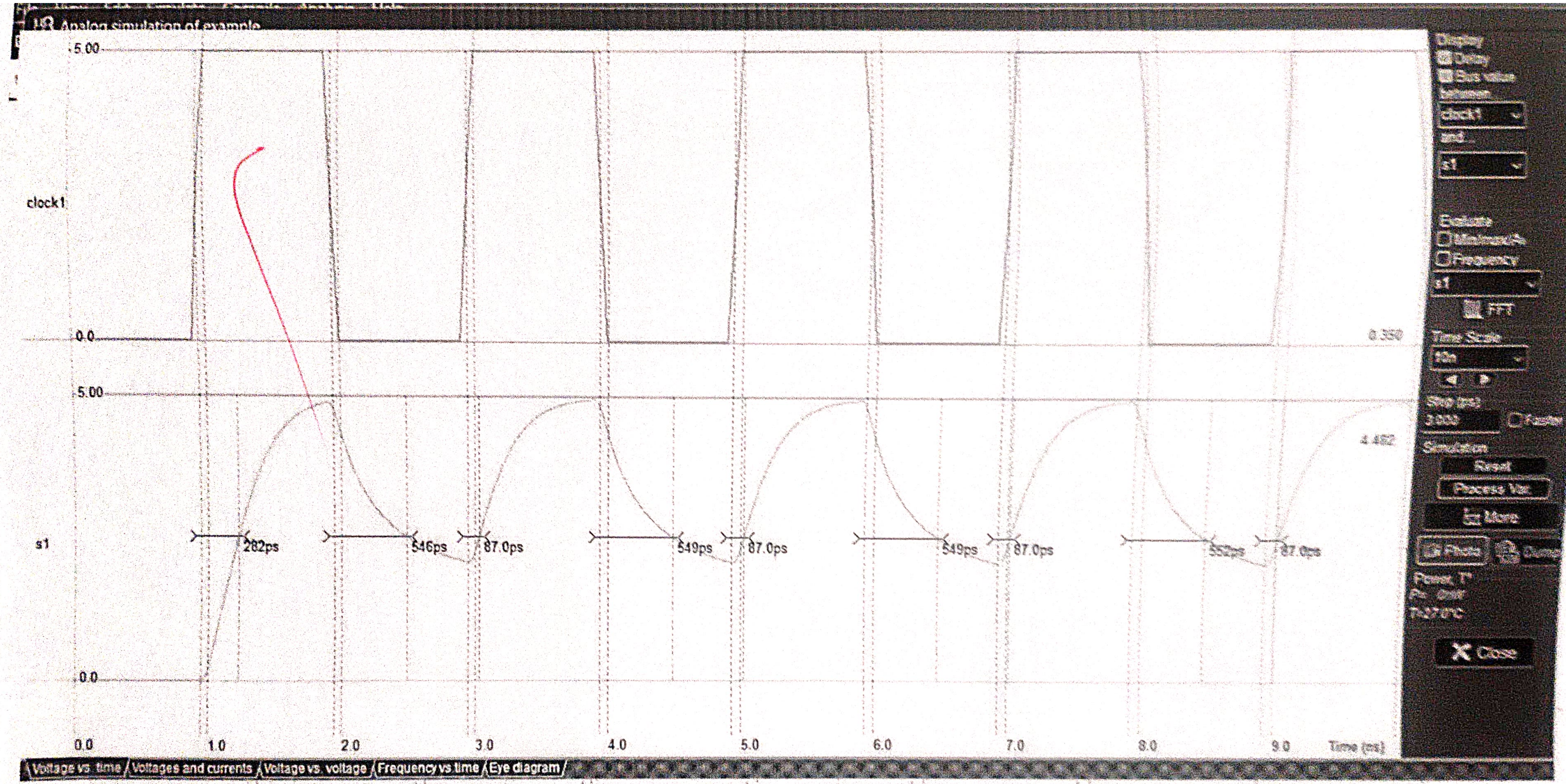


Figure 4.1 Output of NMOS pass transistor.

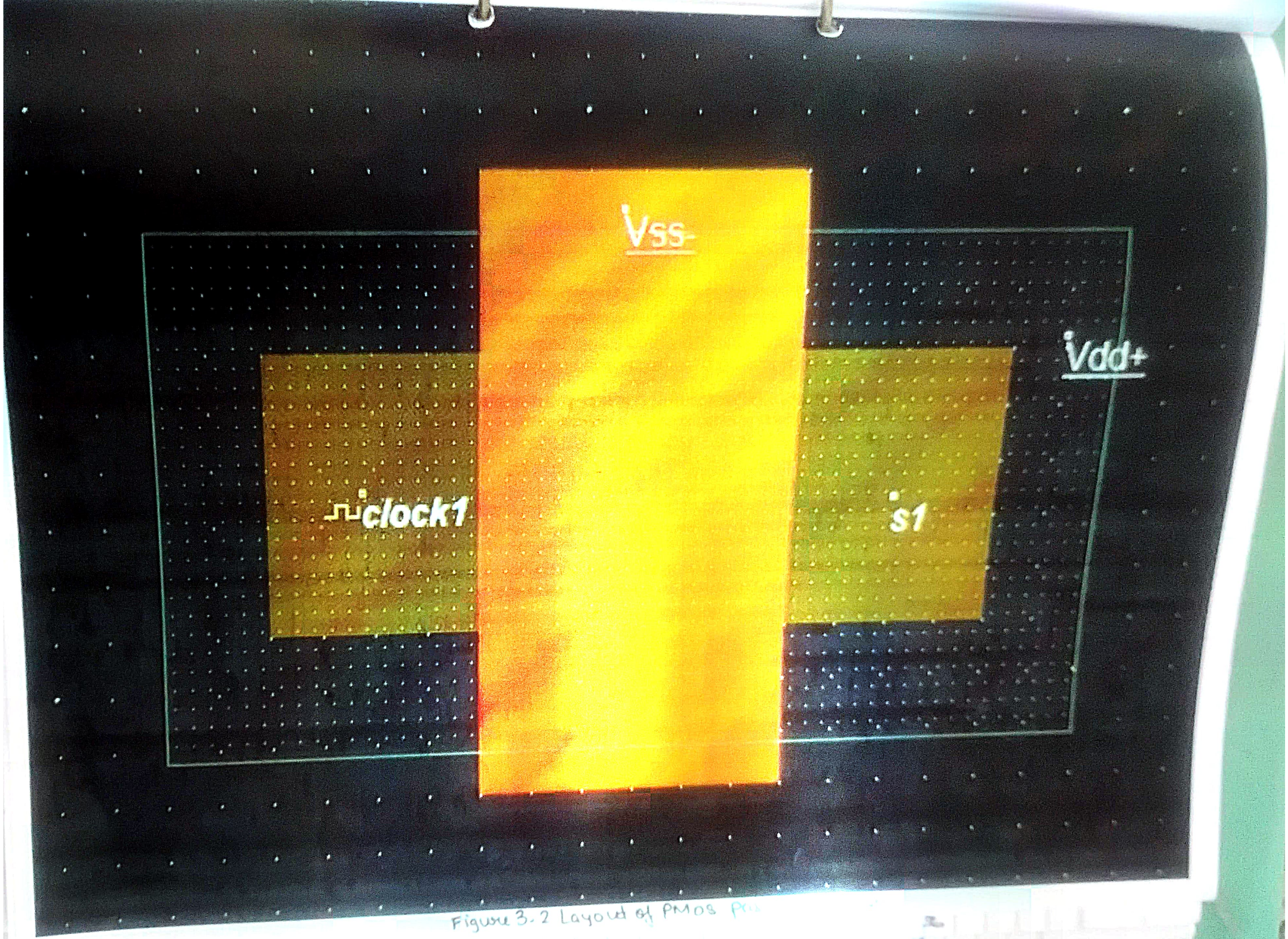


Figure 3.2 Layout of PMOS

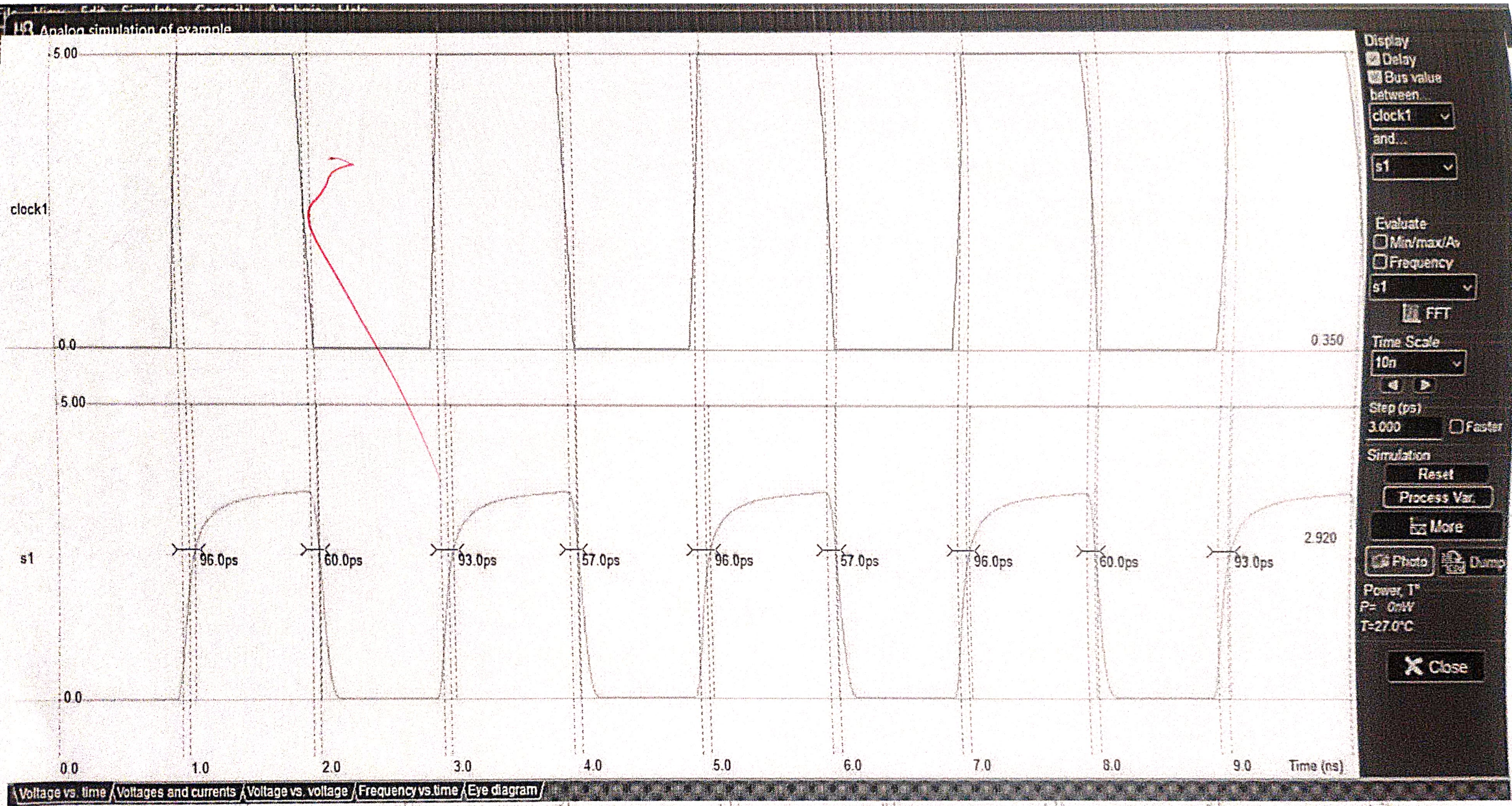


Figure 4.2 Output of PMOS pass transistor.

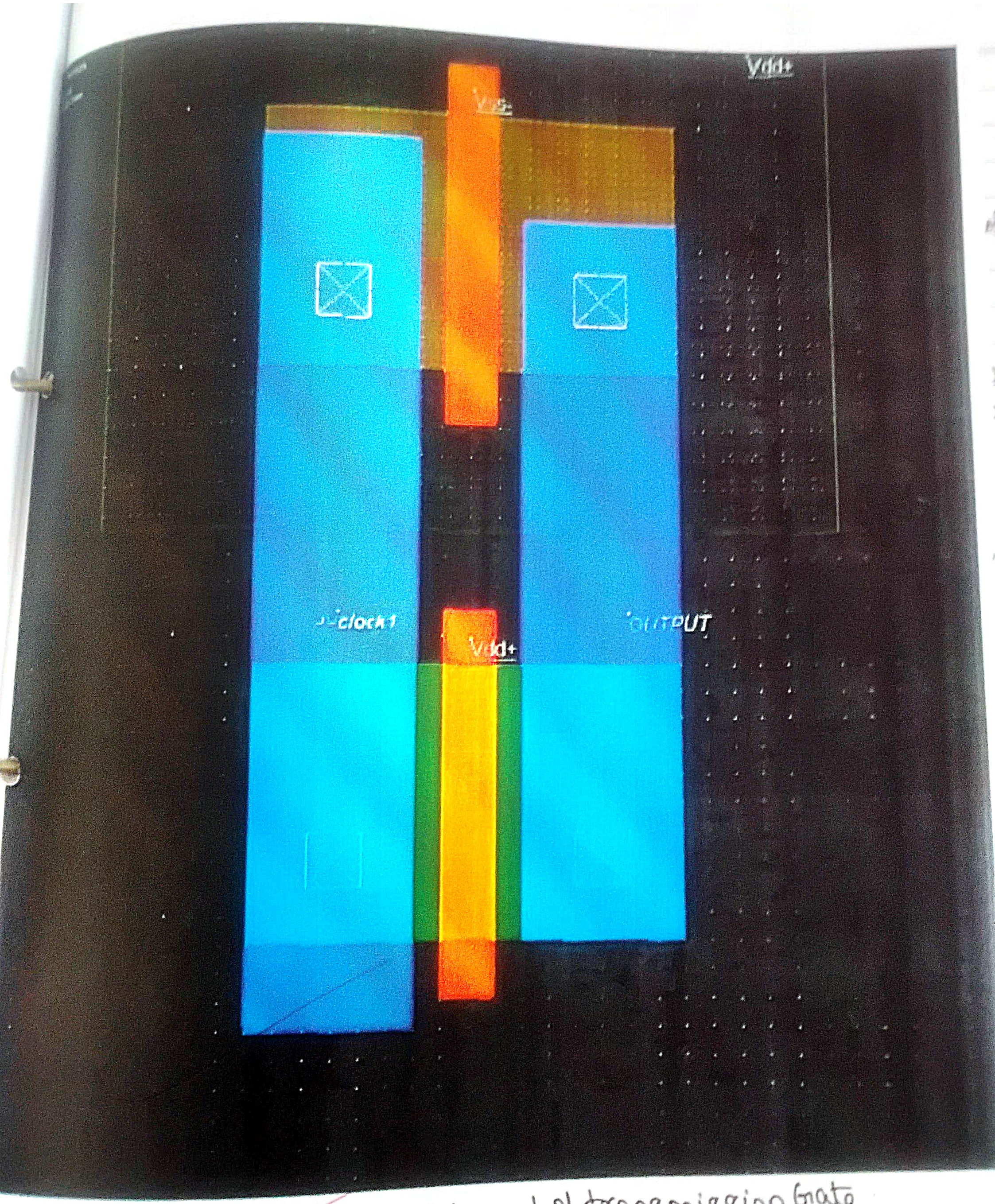


Figure 5. layout of transmission Gate

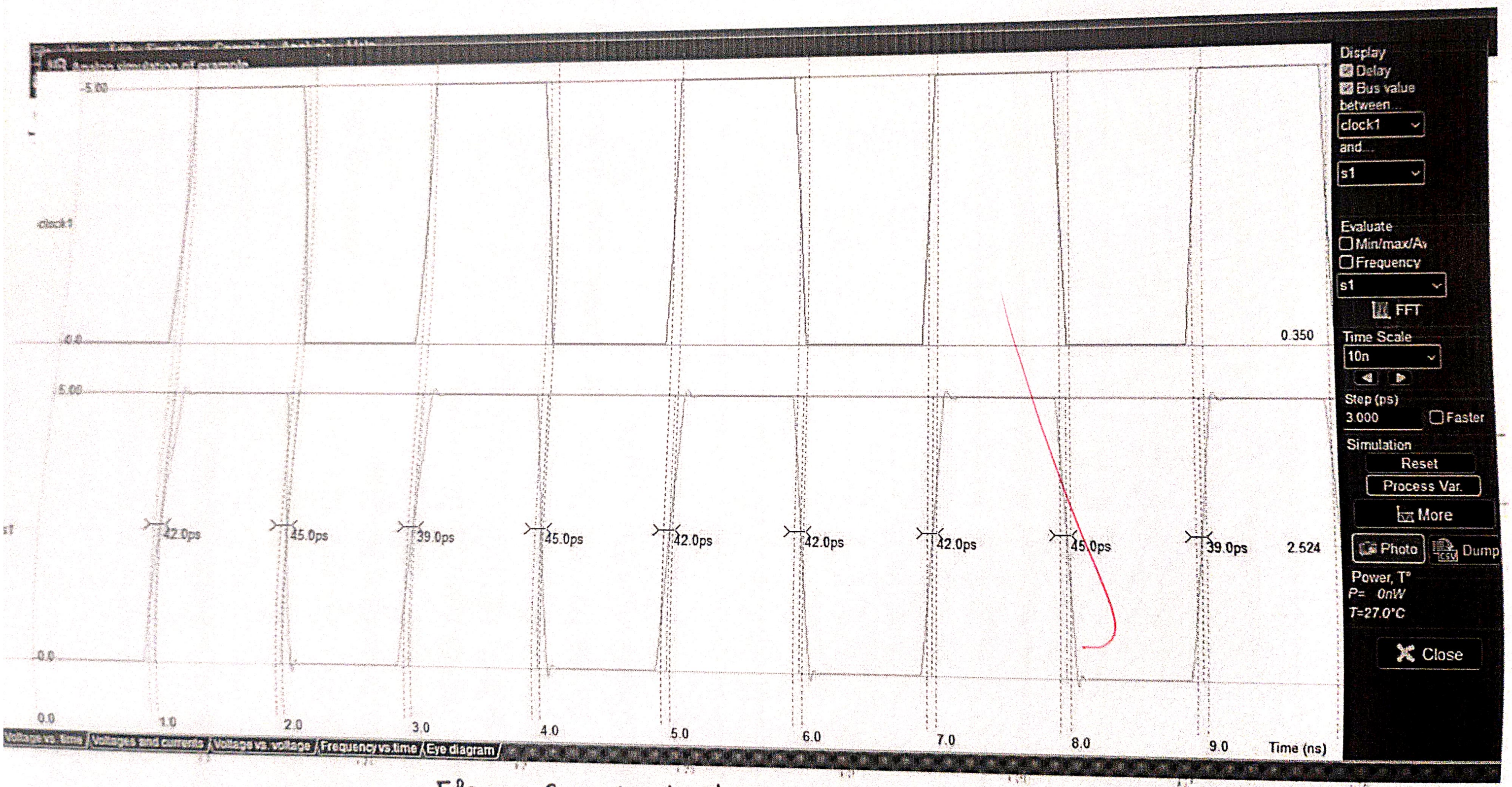
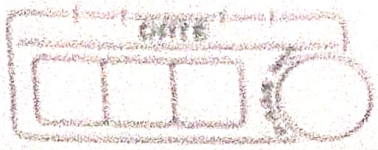


Figure 6. Output of transmission Gate.

Result analysis & conclusion

Pass transistor logic utilizes NMOS and PMOS transistors to transfer changes between circuit nodes under MOS gate control NMOS transistors pass strong 0's & weak 1's, while pmos transistors pass strong 1's & weak 0's. By combining both in transmission gates, strong signals for both 1s & 0s are achieved. This technique is useful in designing multiplexers & ROM's. We have performed this experiment in Microwind By drawing the layers of CMOS using NMOS & PMOS for transmission gate.



Post Experiment Questions :-

Q1] NMOS passes strong 0 & PMOS pass strong 1. Justify.

→ In an NMOS transistor, the source-drain voltage drops when passing a high voltage (1), resulting in a degraded 1. However, it passes a low voltage (0) efficiently due to the lack of ~~drop~~ such drop thus producing a strong 0. Conversely, a PMOS transistor efficiently passes a strong 1 but struggles with passing a due to voltage degradation, resulting in a weaker 0. This justify their behaviour in switching.

Q2) What is advantages of Transmission gate logic?

→ Transmission gate logic offers key advantages such as low power consumption, reduced transistor count & bidirectional signal flow, making it 4 latches. By combining NMOS & PMOS transistors. It ensures strong 0's & 1's minimizing voltage degradations. This results in faster switching & higher reliability especially in low-power & high-speed digital circuits.

8/10/24

09/10

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

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Evaluation

Performance Indicator	Max. Marks	Marks Obtained
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Understanding	5	04
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Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

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Name of Faculty:

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Date:

8/10/24

Experiment No: 13

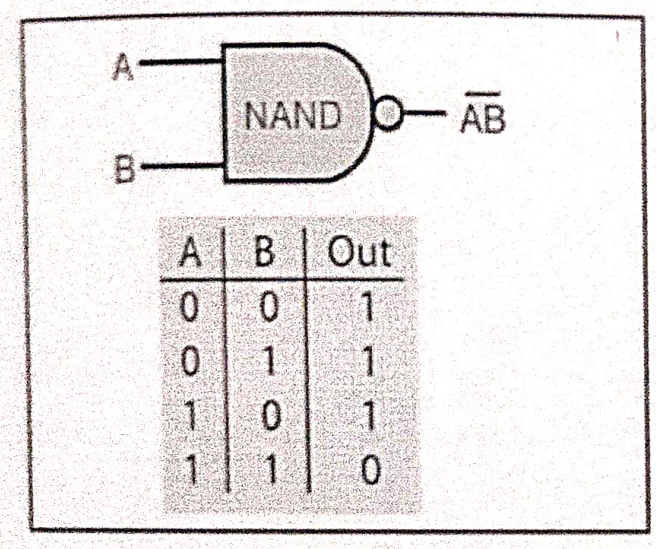
Aim: To Sketch Layout of NAND and NOR gates using Microwind.

Software: MICROWIND 3.8

Theory:

NAND Gate

The logic or Boolean expression given for a logic NAND gate is that for *Logical Addition*, which is the opposite to the AND gate, and which it performs on the *complements* of the inputs. The Boolean expression for a logic NAND gate is denoted by a single dot or full stop symbol, (.) with a line or *Overline*, (¯) over the expression to signify the NOT or logical negation of the NAND gate.



A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

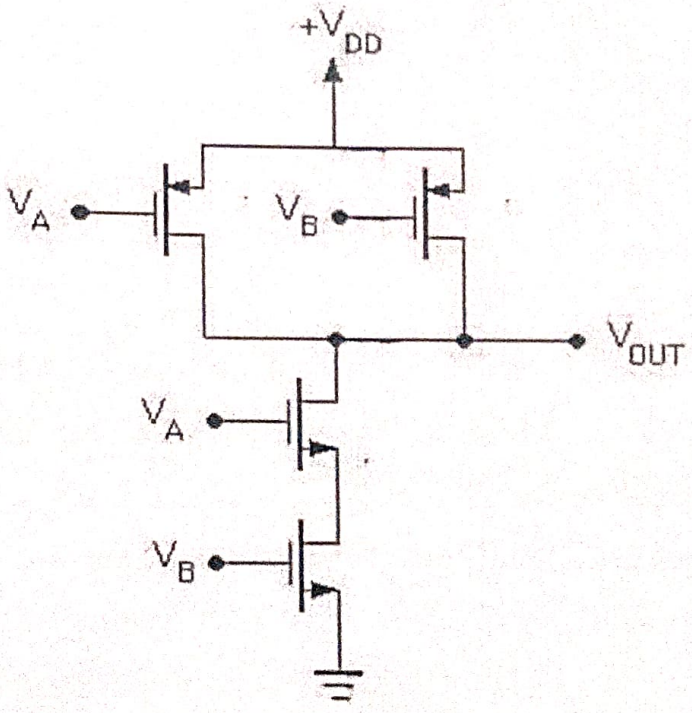


Figure.1 CMOS Realization of NAND gate and its truth table

CMOS implementation of a two-input NAND gate consist of pull-down sub-circuit made of a series combination of two NMOS transistors as shown in figure1. These are responsible for conducting logic '0' to the output node when both of the gates are at logic '1'. The pull-up path on the other hand consists of a parallel combination of two PMOS transistors. If either of the logic is `0', the output node assumes the value `1'.

II NOR Gate:

The logic or Boolean expression given for a logic NOR gate is that for *Logical Multiplication* which it performs on the *complements* of the inputs. The Boolean expression for a logic NOR gate is denoted by a plus sign, (+) with a line or *Overline*, (¯) over the expression to signify the NOT or logical negation of the NOR gate.

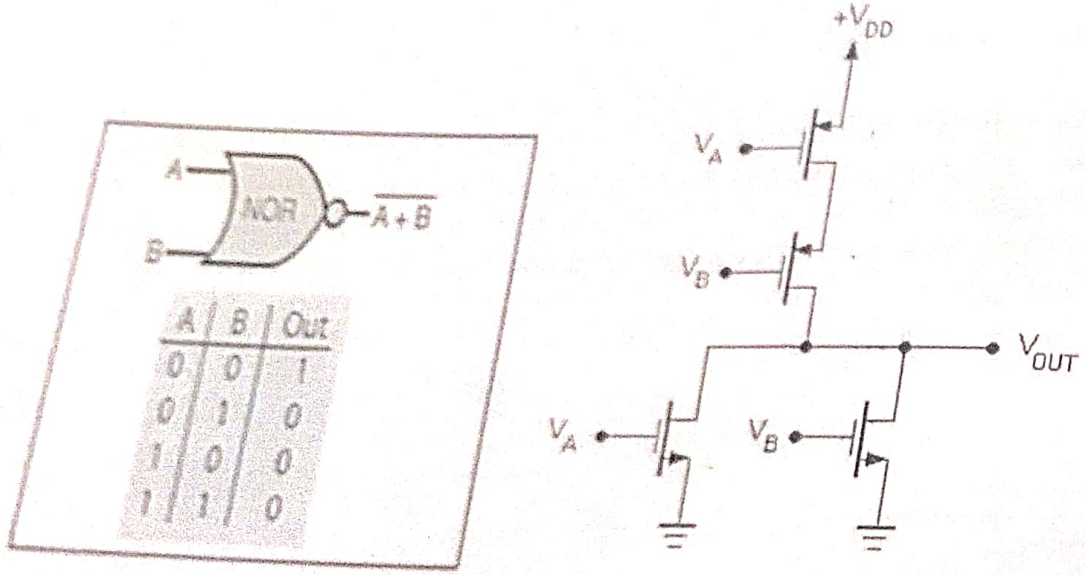
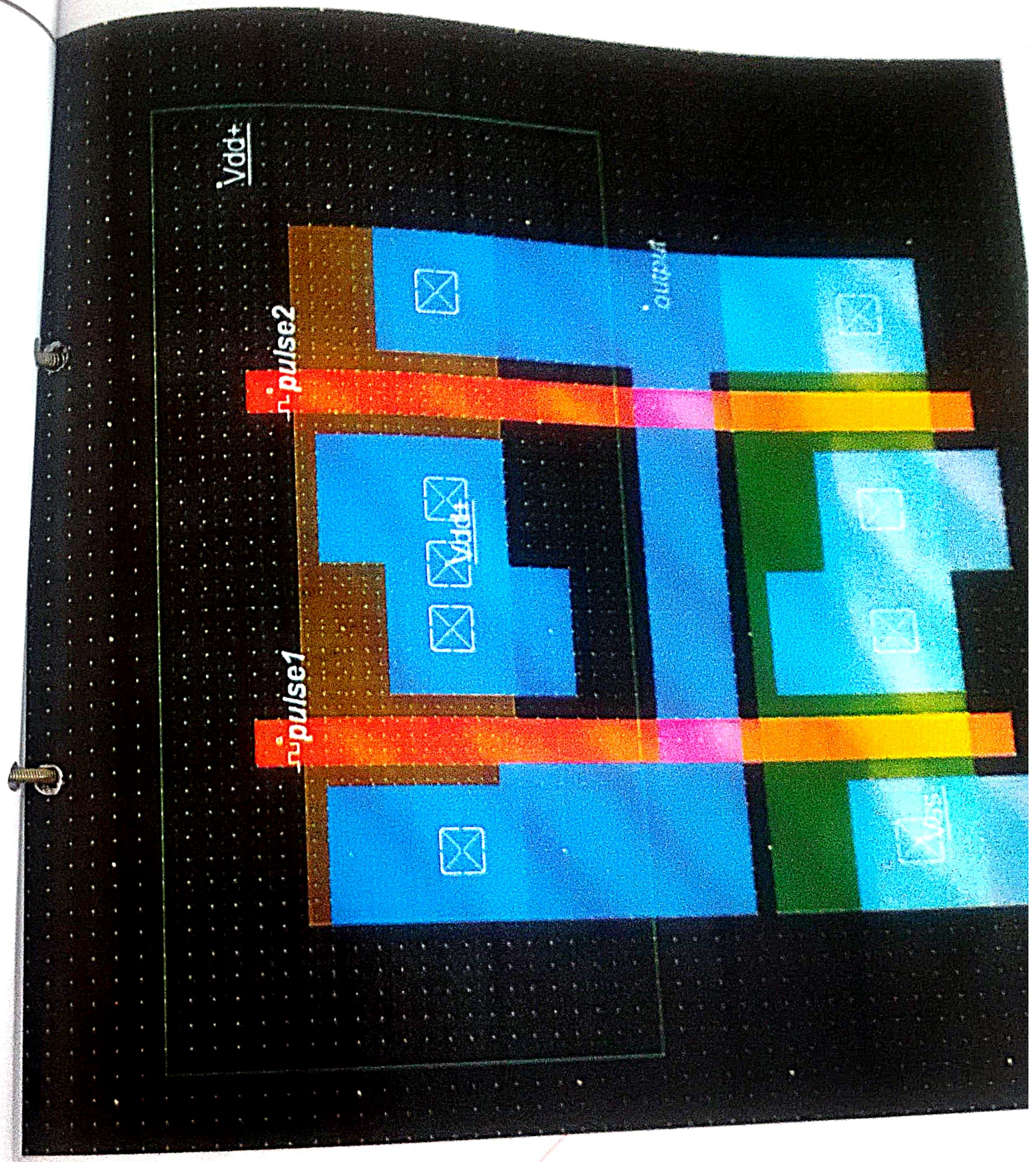


Figure.2 CMOS Realization of NOR gate and its truth table

CMOS implementation of a two-input NOR gate consists of pull-up sub-circuit made of a series combination of two PMOS transistors as shown in figure 2. These are responsible for conducting logic '1' to the output node when both of the gates are at logic `0'. The pull-down path on the other hand consists of a parallel combination of two NMOS transistors. If either of the logic is '1', the output node assumes the value `0'.

Procedure:

1. Select the foundry.
2. Draw the layout using palette according to lambda based design rules in microwind tool.
3. Apply appropriate supply voltage and Input signal.
4. Connect the visible node to observe output.
5. Check layout with design rule checker for any design rule violation
6. Simulate the circuit from Microwind tool.
7. Check the functionality of circuit using the truth table.



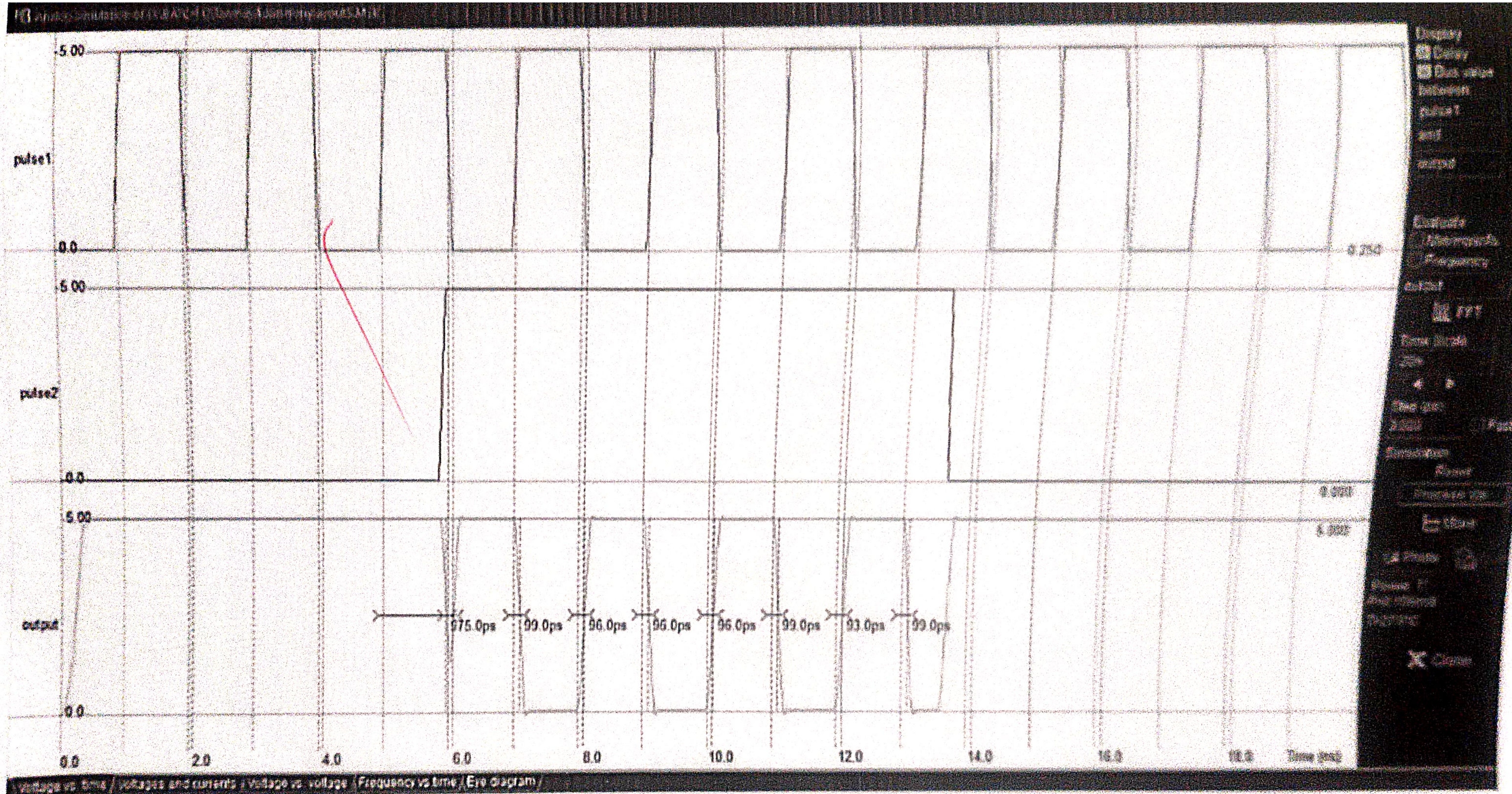


Figure 5. output of NAND gate

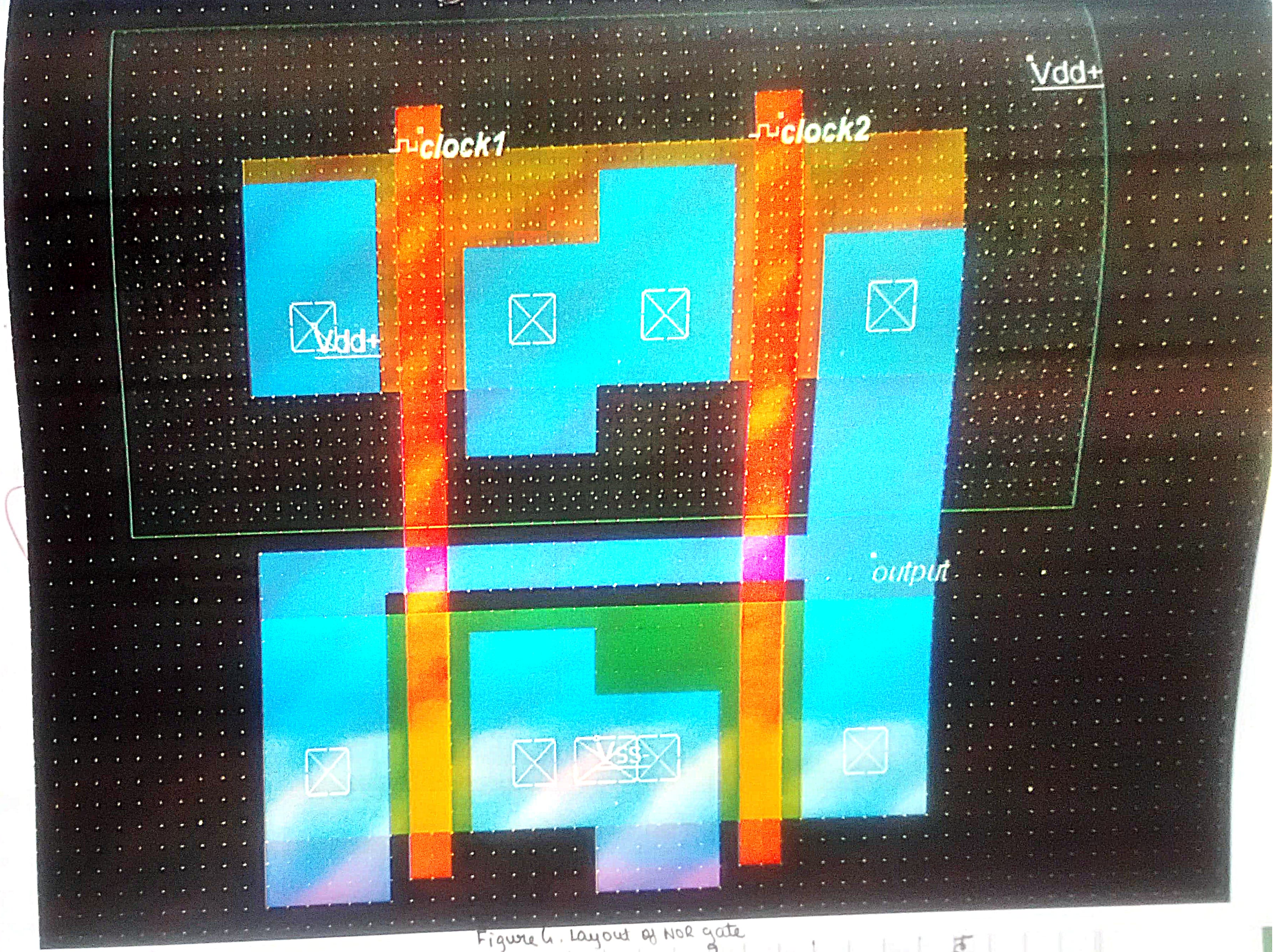


Figure 6. Layout of NOR gate

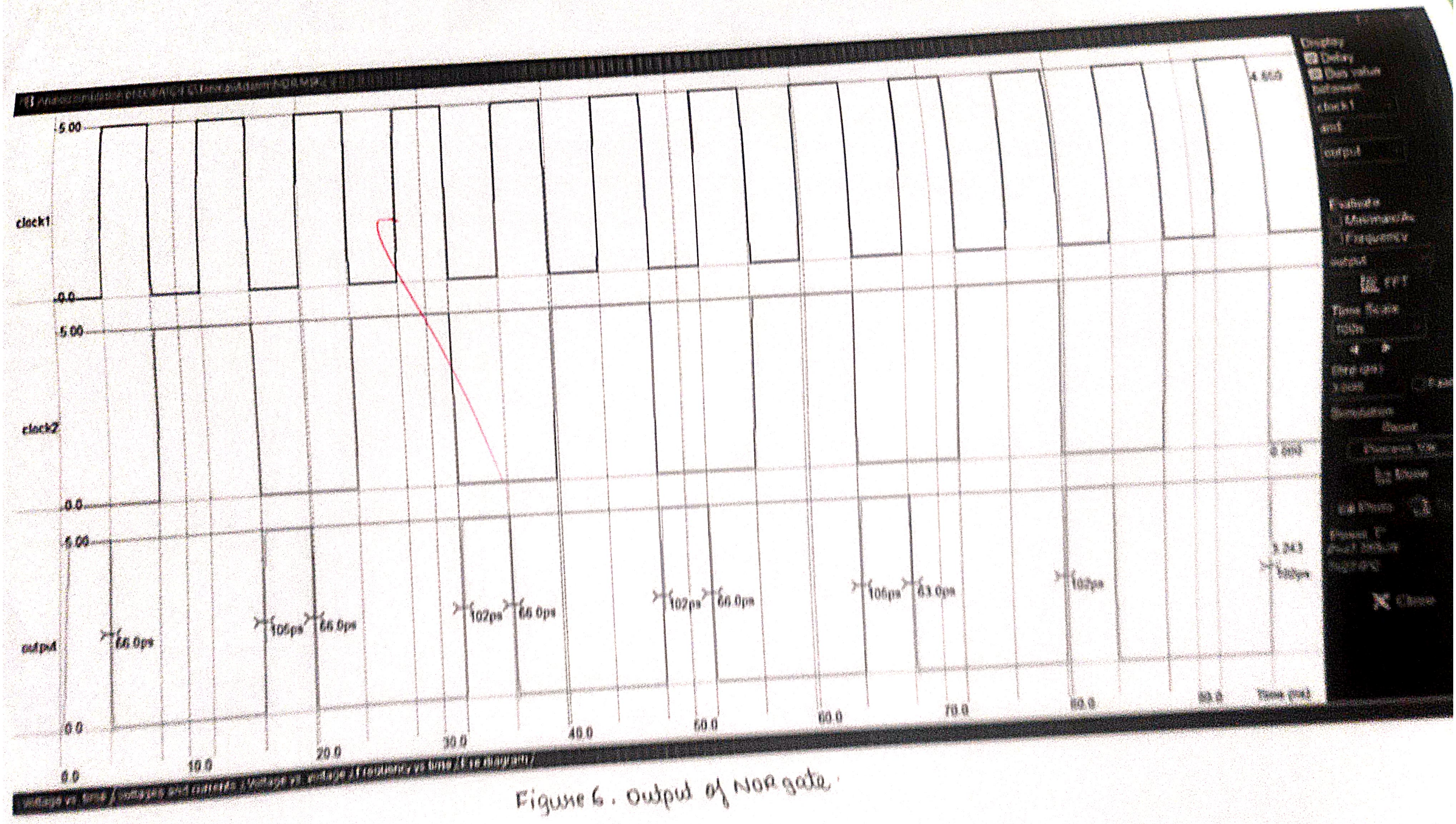


Figure 6. Output of Nor gate.

Result analysis & conclusion

The NAND and NOR gates were successfully designed & simulated using Microwind. Both gates followed CMOS logic, with the NAND gate outputting 0 only when both inputs were 1, & the NOR gate outputting only when both inputs were 0. The layouts were created following lambda-based rule with no design rule violations detected. Simulations confirmed the expected behavior, validating the use of CMOS technology for reliable logic gate implementation. This experiment highlights the significance of NAND & NOR gates as universal gates in digital logic design.

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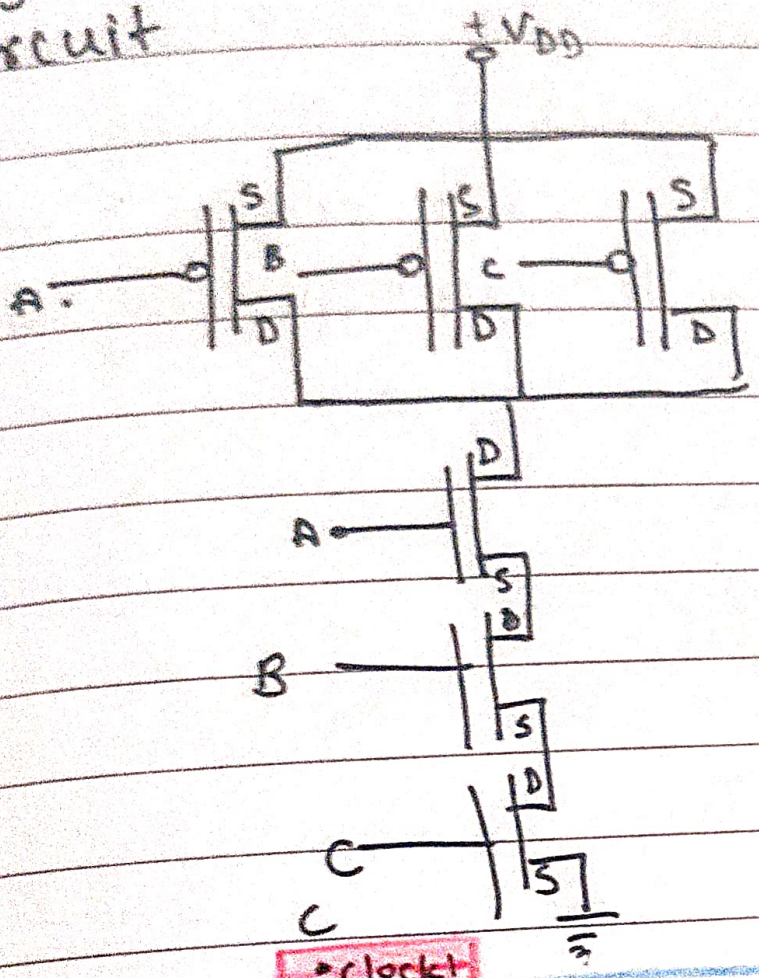
Post Experiment Questions:

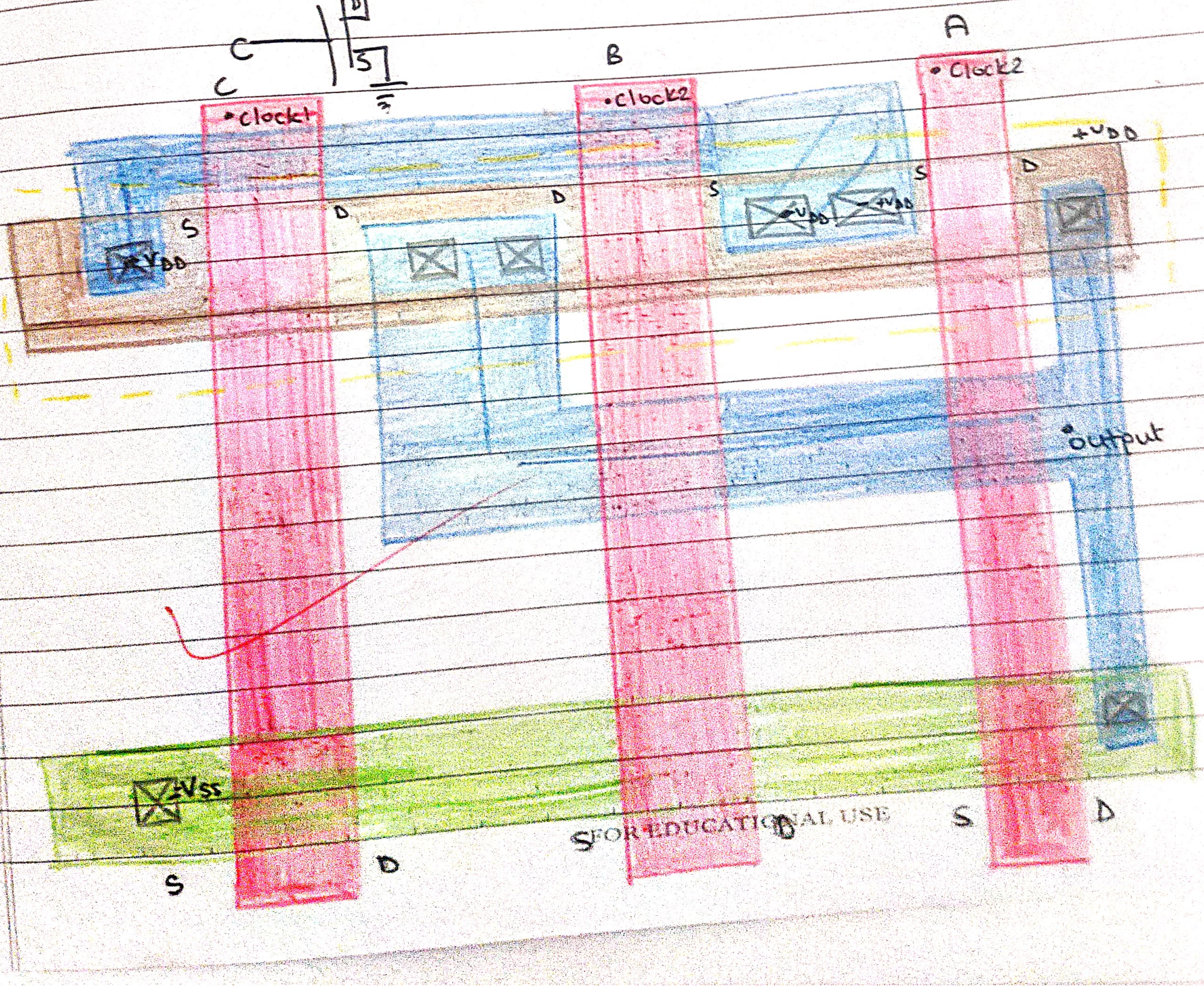
a) Draw circuit & layout for 3 input NAND.

→ $y = \overline{A \cdot B \cdot C}$

Circuit



Layout



Q2) How to reduce area of layout as number of input increase

→ To reduce the layout area as the number of input increases use techniques like transistor sizing to minimize unnecessary space, optimize the use of shared diffusion regions & apply multi input gates to reduce transistor count. Employing advanced layout techniques such as gate merging minimizing interconnect lengths & using compact design rules can also enchance area efficiency while maintaining performance.

8/10/24 09/10

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmayi Umesh Upadhya
Roll No. :	48
Practical No.:	14
Title of Practical:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	4
Journal work and timely submission	10	09
Total	20	18

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

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Name of Faculty:

Signature:

Date:

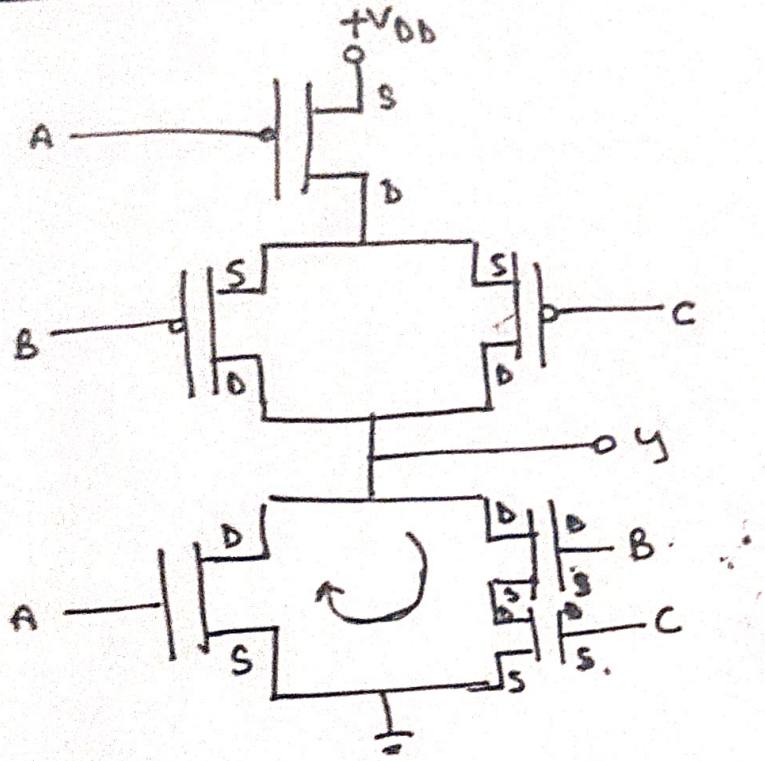
8/10/24

Experiment No: 14

Aim: Realize and draw layout any expression using any logic style, using Microwind.

Software: MICROWIND 3.8

Circuit realization: $Y=\overline{A+BC}$



Truth Table:

A	B	C	Y=A+BC'
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Procedure:

1. Select the foundry.
2. Draw the layout using palette according to lambda-based design rules in microwind tool.
3. Apply appropriate supply voltage and Input signal.
4. Connect the visible node to observe output.
5. Check layout with design rule checker for any design rule violation
6. Simulate the circuit from Microwind tool.
7. Check the functionality of circuit realized.

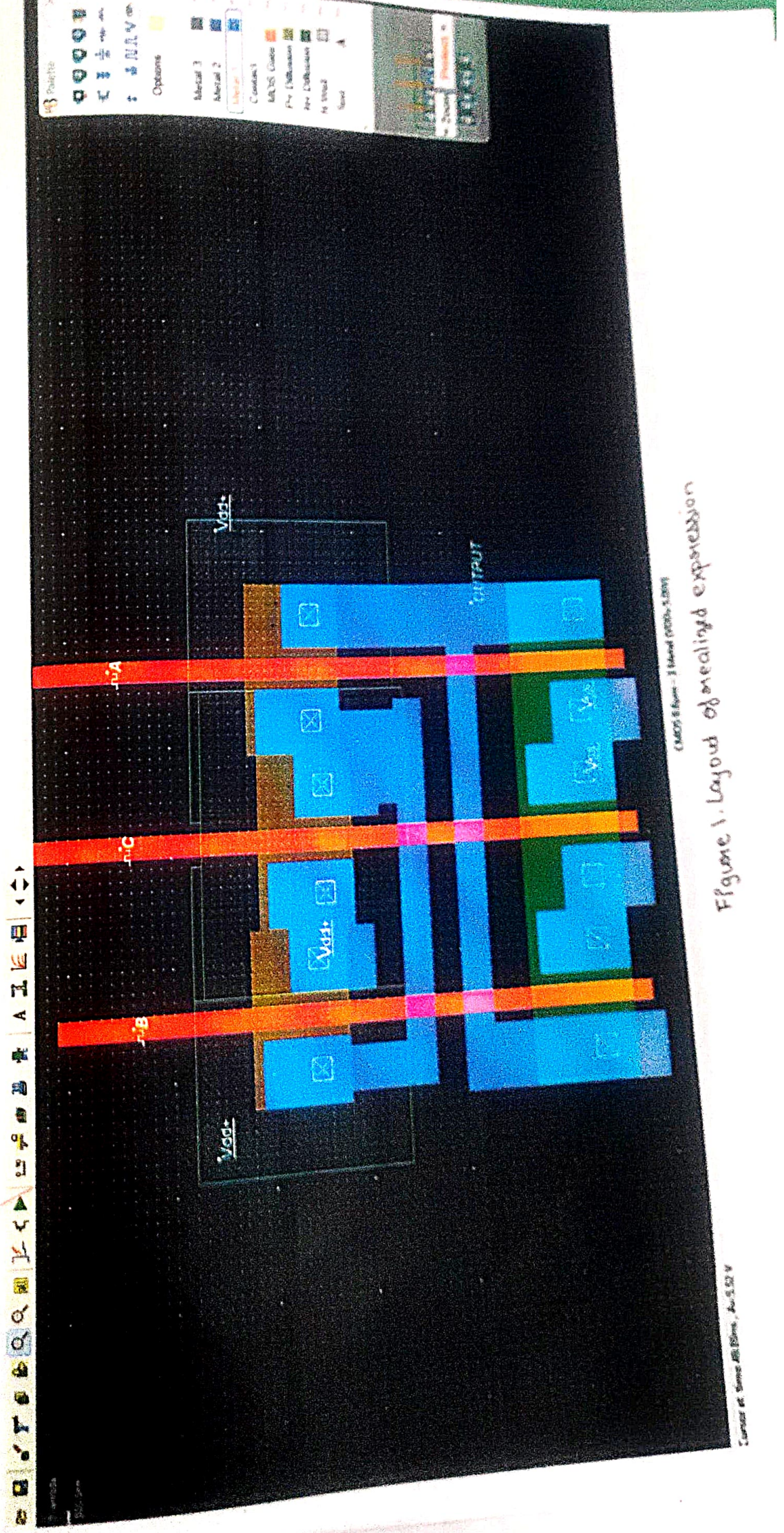


Figure 1. Layout of NAND gate expression

Result analysis and conclusion:-

The chosen logic expression was successfully implemented using microwind. following using design rules and layout procedures. The circuit was designed, simulated & verified for its intended functionality. The design adhered to the lambda-based rules and the layout passed the design rule checker without violations. The circuits output was consistent with the expected logic behaviour.

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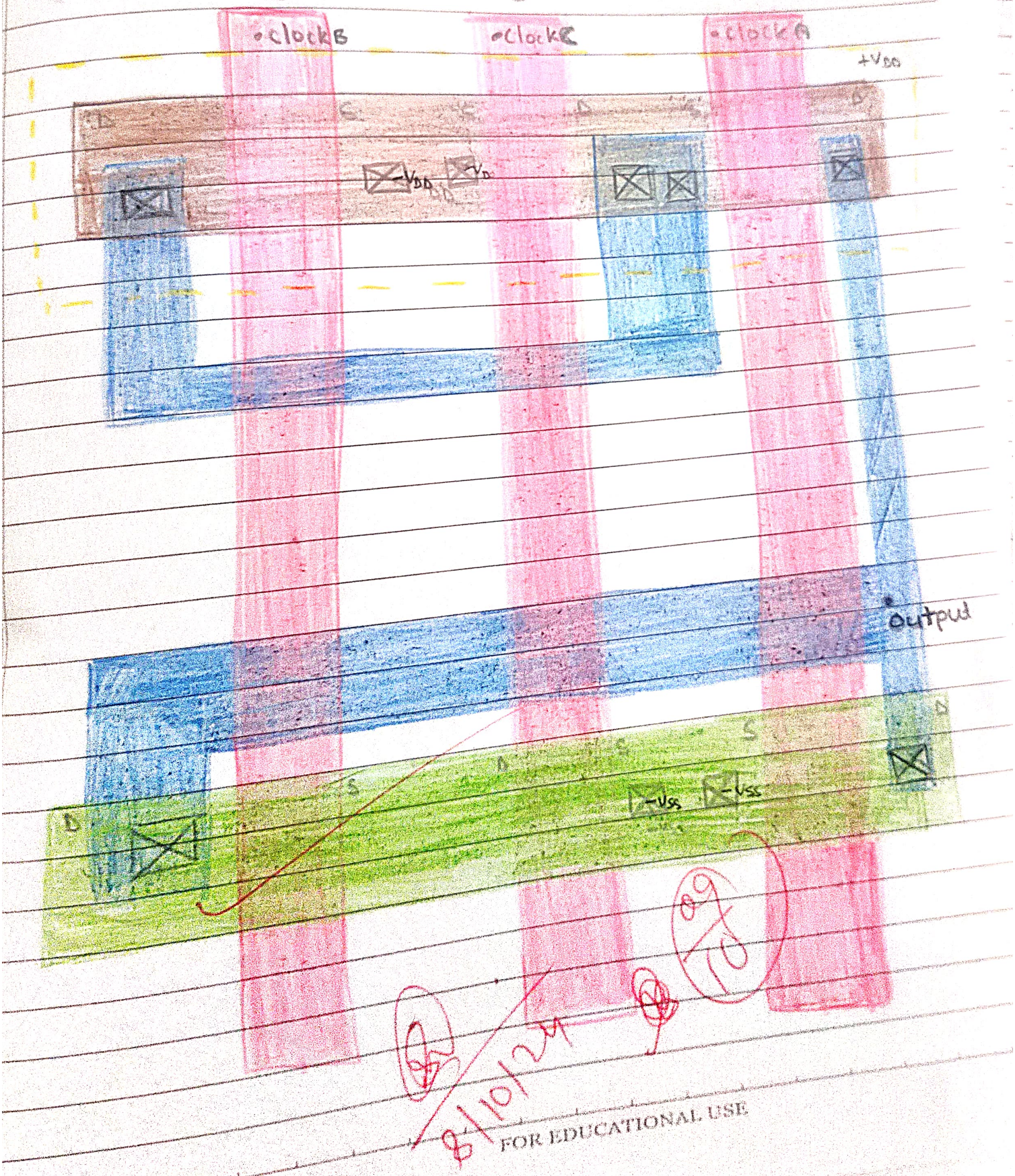
Post Experiment Questions:-

Draw layout of realized circuit using LAMBDA rules



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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmayi Umesh Upadhya
Roll No:	48
Practical No:	05
Title of Practical:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Performance	5	05
Understanding	5	04
Journal work and timely submission	10	09
Total	20	18

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Performance	4-5	2-3	1-2
Understanding	4-5	2-3	1-2
Journal work and timely submission	8-10	6-7	2-3

Checked by

Name of Faculty:

Signature:

Date:

17/10/24

Experiment No: 15

Aim: To implement half adder using LT Spice and draw layout, verify the truth table.

Software: Microwind 3.8

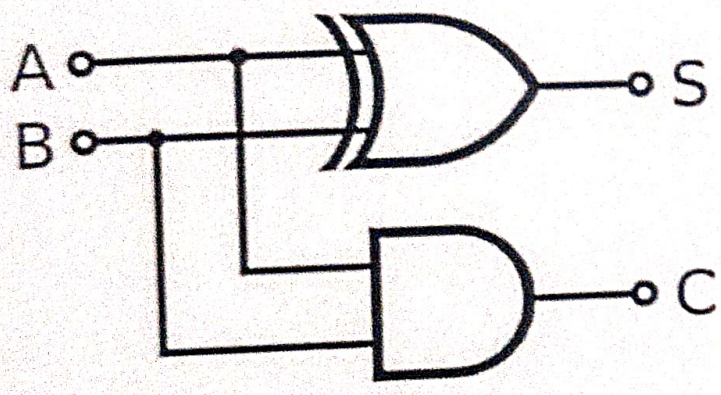
Theory: An adder is a kind of calculator that is used to add binary number. It can be integrated with many other circuits for a wide range of applications. There are of two kinds of adders:

1. Half adder
2. Full adder

Half Adder: The half adder consists of two input variables designated as Augends and Addend bits as shown in figure1. Output variables produce the Sum and Carry. The 'carry' output is 1 only when both inputs are 1 and sum is 1 if any one input is 1. The Boolean expression is given by,

Sum = x ^ y

Carry = x & y



Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure.1 Half Adder Gate level realization and Truth table

Procedure:

For Microwind:

1. Select the foundry.
2. Draw the layout using palette according to lambda based design rules in microwind tool.
3. Apply appropriate supply voltage and Input signal.
4. Connect the visible node to observe output.
5. Check layout with design rule checker for any design rule violation
6. Simulate the circuit from Microwind tool.
7. Check the functionality of circuit and voltage levels.

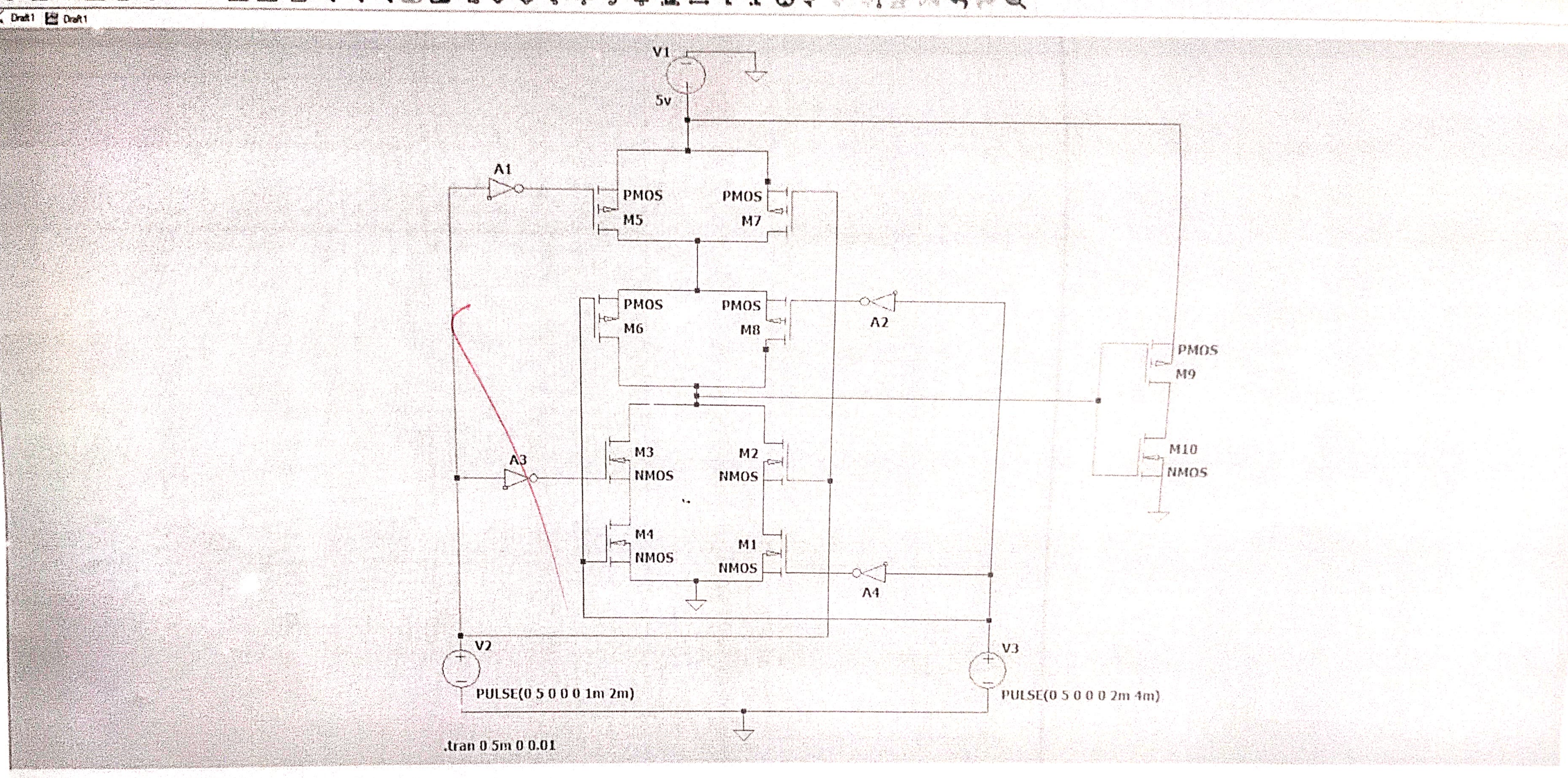


Figure 2. Realization of SOM circuit using CMOS logic.

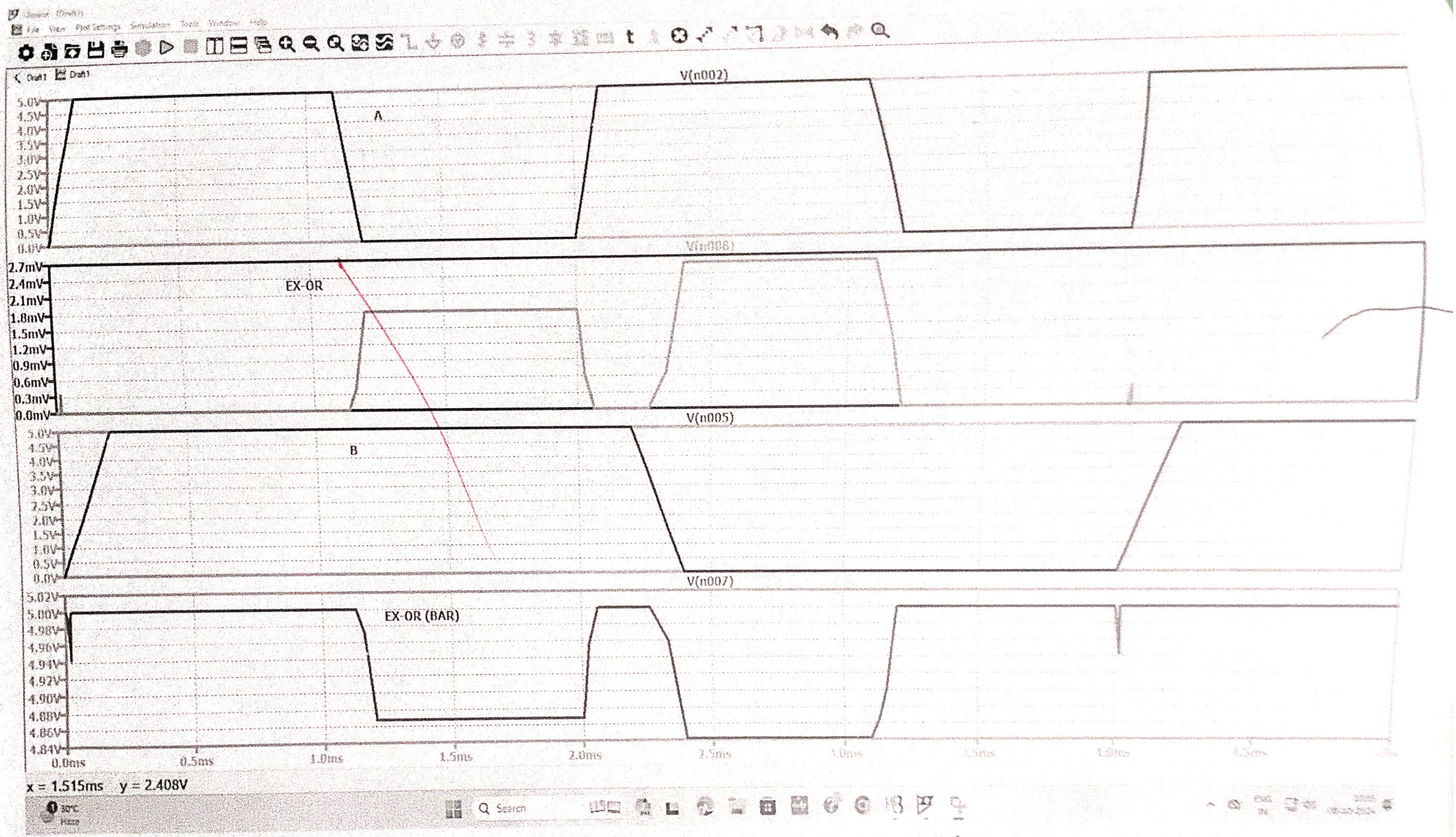


Figure 3. output of SUM circuit using CMOS logic.

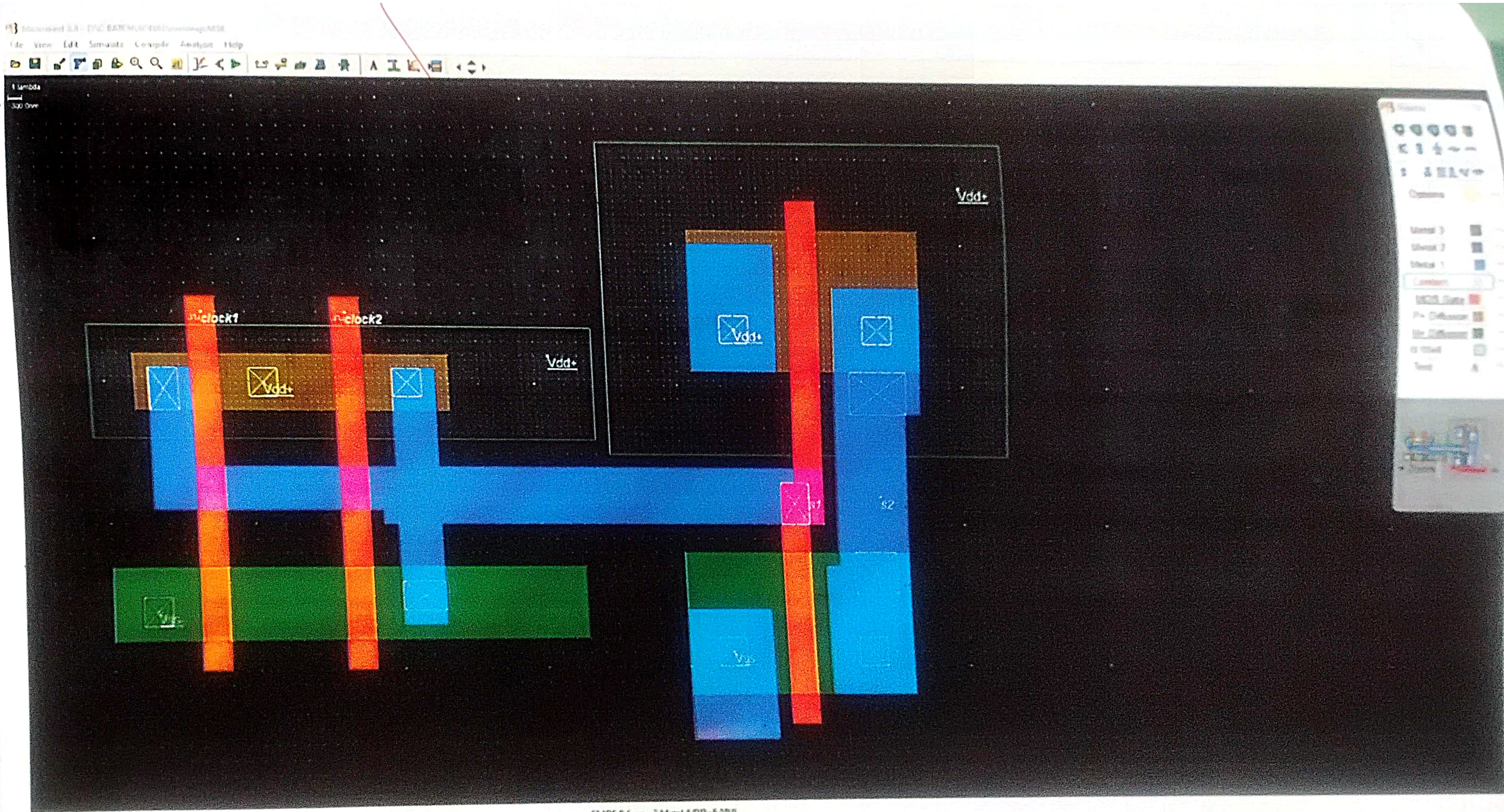


figure 4.1 layout of Carry circuit using CMOS logic

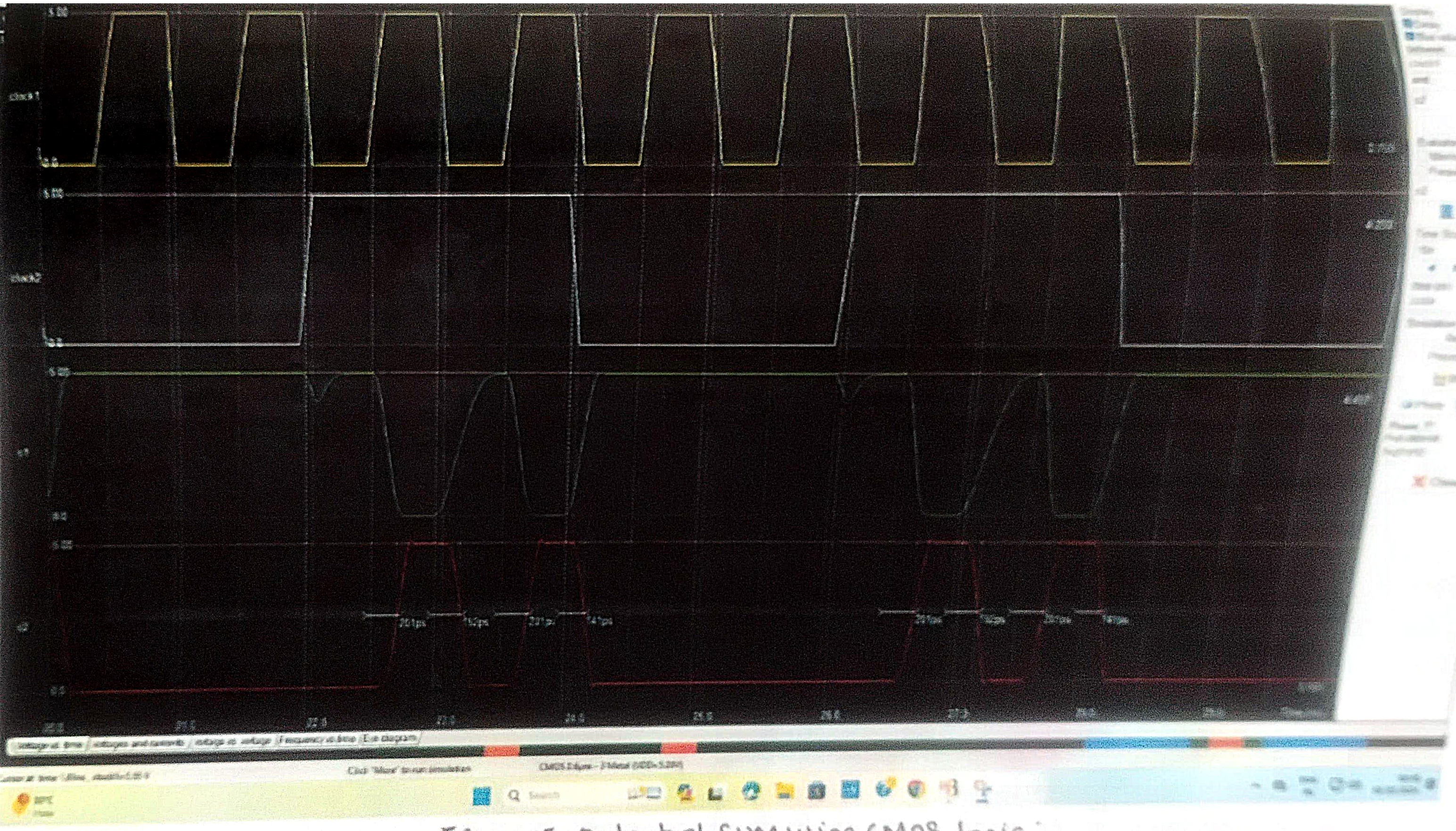


Figure 5. Output of SUM using CMOS logic

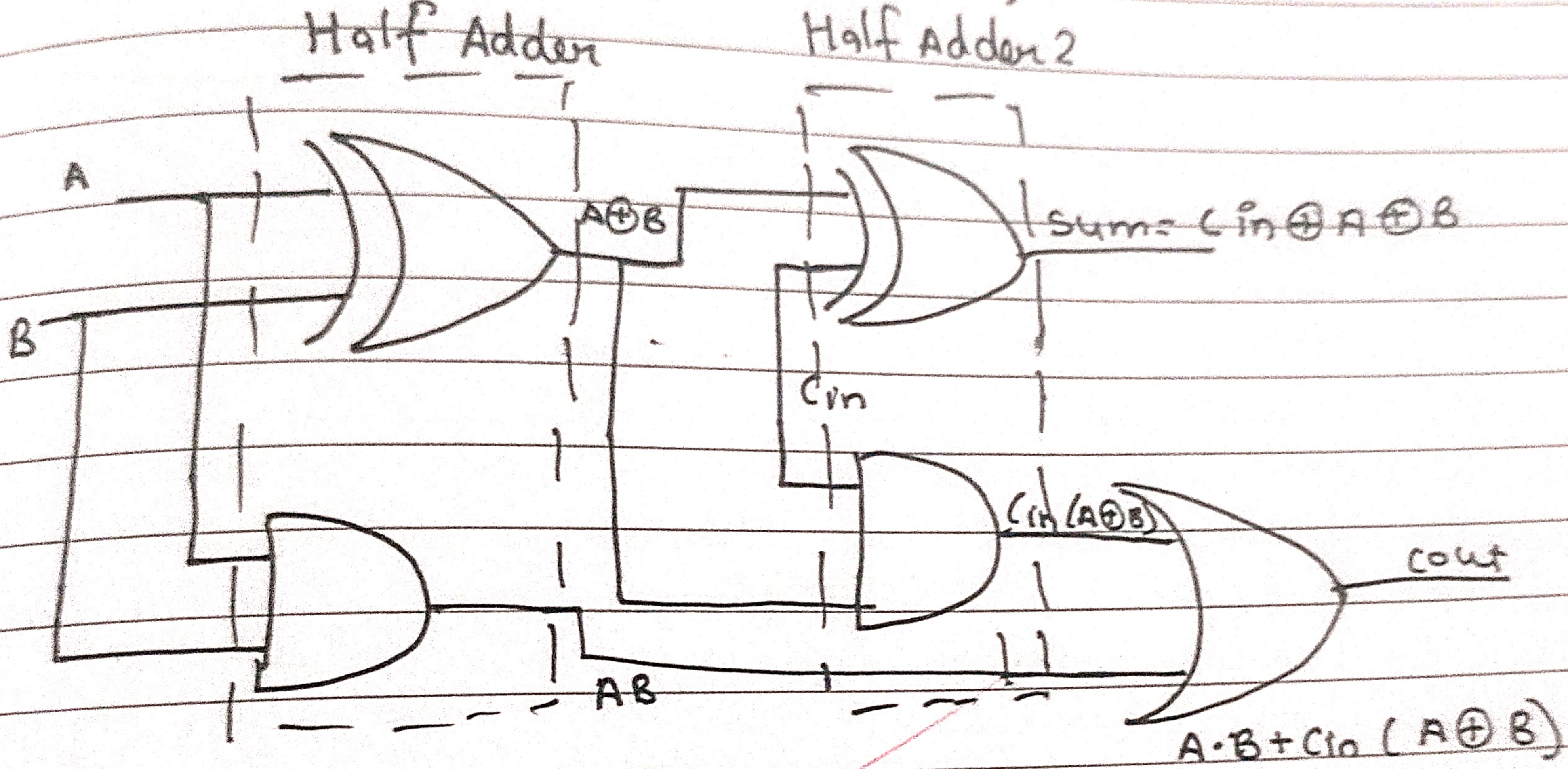
Result analysis & conclusion:

The half adder circuit was successfully designed & simulated using both LTspice and microwind. The circuit accurately performed binary addition, producing the correct Sum & Carry outputs as per the truth table. The XOR gate generated the SUM, while the AND gate generated the carry output. In microwind, the layout was designed following lambda-based design rules, with no violations detected during the design rule check (DRC). The simulation confirmed the expected logic functionality at all voltage levels. Similarly, the LTSpice simulation verified the correctness of the circuit by matching the simulated outputs with the theoretical truth table. This experiment demonstrates the practical implementation of a half adder, which serves as a building block for more complex circuits like full adders used in digital arithmetic systems

Post Experiment Questions:-

Q1) Realize full adder using half adder?

→



09/10

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmayi Umesh Upadhya
Roll No.:	48
Assignment No.:	01
Title of Assignment:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Legibility	4	04
Demonstrated Knowledge	4	03
Timely submission	2	02
Total	10	9

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Legibility	4	2-3	1-2
Demonstrated Knowledge	4	2-3	1-2
Timely submission	2	1	1

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Name of Faculty:

Signature:

Date:

Name: chinmay' Umesh Upadhya
Rollno: 48

Assignment 1

Q1) For n-channel MOSFET

→ $V_{GS} = V_G - V_S = 5V - 2V = 3V$; $V_{DS} = V_D - V_S = 7 - 2 = 5V$

→ $V_{DSsat} = V_{GS} - V_T$

$= 3V - 0.8V$

$V_{DSsat} = 2.2V$

$\therefore V_{DS} > V_{DSsat}$

$\therefore$ It is in Saturation region with Channel length Modulation

$$I_{D(sat)} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$= \frac{20 \times 10^{-6}}{2} \frac{10}{1} (2.2)^2 (1 + 0.04 \times 5)$$

$$= 1.1616 \times 10^{-3}$$

$\boxed{I_{D(sat)} = 1.1616 mA.}$

→Q2) $P = V_{DS} \cdot I_D$

$P' = V_{DS}' \cdot I_D'$

$P' = \frac{V_{DS}}{S} \cdot \frac{I_D}{S^2}$

$\boxed{P' = \frac{P}{S^2}}$

$I_D' = k_p' (V_{GS} - V_T)^2$

$= Sk_p \left(\frac{V_{GS}}{S} - \frac{V_T}{S}\right)^2$

$I_D' = \frac{Sk_p I_D}{S}$

$\therefore$ Power consumption is less by S^2 factor.

→Q3)

Oxide Capacitance in Satn	Oxide Capacitance in linear region
① $WL_g C_{ox}$ - by Overlap Capacitance	① $WL_g C_{ox}$ - by Overlap Capacitance
② $\frac{2}{3} WL C_{ox}$ - by C_{gs}	② $\frac{1}{2} WL C_{ox}$ - by C_{gs}
③ $C_{gd} = 0$	③ $\frac{1}{2} WL C_{ox}$ - by C_{gd}.
④ $C_{gb} = 0$	④ $C_{gb} = 0$.
① here C_{gs} is ~~only~~ present as depletion layer is found near G_{TO}	① here C_{gb} is not there has channel divides C_{gb}.

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVLSI

Name of Student:	Chinmayi Umesh Upadhya
Roll No.:	48
Assignment No.:	02
Title of Assignment:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Legibility	4	04
Demonstrated Knowledge	4	04
Timely submission	2	02
Total	10	10

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Legibility	4	2-3	1-2
Demonstrated Knowledge	4	2-3	1-2
Timely submission	2	1	1

Checked by

Name of Faculty:

Signature:

Date:

Name ... Upadhya

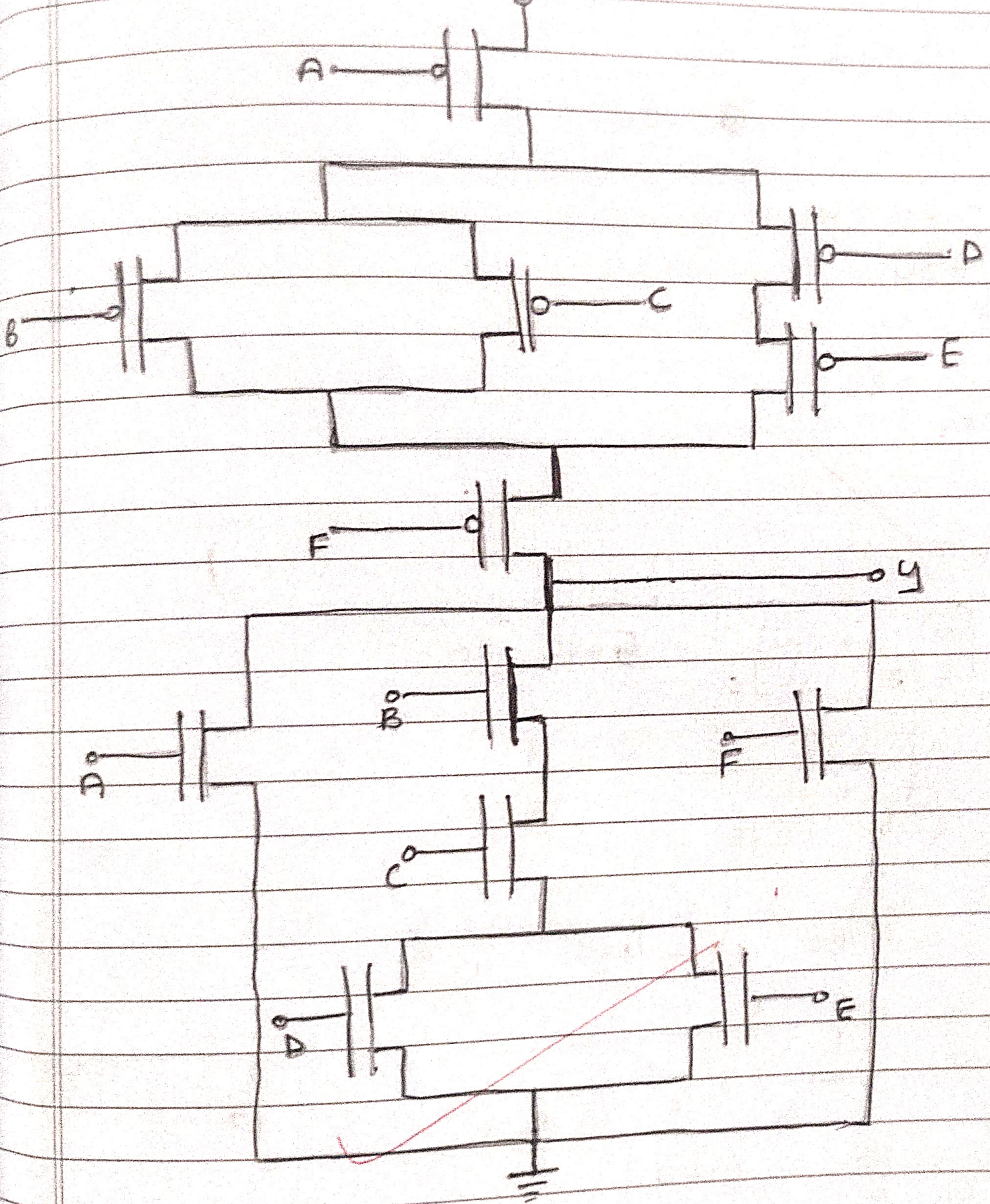
Rollno: 48.

Assignment 2.

Q. Draw the CMOS circuit for $y = \overline{A+BC(D+E)+F}$ & find equivalent CMOS Inverter for simultaneously switching of all Input

Assume $\left(\frac{W}{L}\right)_P = 15$ $\left(\frac{W}{L}\right)_N = 10$

→ $y = \overline{A+BC(D+E)+F}$



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for eq.(n)

$$\left(\frac{\omega}{L}\right)_{BC} = \left(\frac{\omega}{L}\right)_B + \left(\frac{\omega}{L}\right)_C = \frac{1}{\frac{1}{10}+\frac{1}{10}} = 5$$

$$\left(\frac{\omega}{L}\right)_{DE} = \left(\frac{\omega}{L}\right)_D + \left(\frac{\omega}{L}\right)_E = 10+10 = 20$$

$$\left(\frac{\omega}{L}\right)_{eq.(n)} = \left(\frac{\omega}{L}\right)_A + \left(\frac{\omega}{L}\right)_F + \frac{1}{\frac{1}{\left(\frac{\omega}{L}\right)_{BC}} + \frac{1}{\left(\frac{\omega}{L}\right)_{DE}}}$$

$$= 10+10+\frac{1}{\frac{1}{5}+\frac{1}{20}}$$

$$= 20+4$$

$$\left(\frac{\omega}{L}\right)_{eq.(n)} = 24.$$

$$\therefore \left(\frac{\omega}{L}\right)_{neq} = 24.$$

for peq.

$$\left(\frac{\omega}{L}\right)_{BC} = \left(\frac{\omega}{L}\right)_B + \left(\frac{\omega}{L}\right)_C = 15+15 = 30$$

$$\left(\frac{\omega}{L}\right)_{DE} = \frac{1}{\frac{1}{\left(\frac{\omega}{2}\right)_D} + \frac{1}{\left(\frac{\omega}{L}\right)_E}} = \frac{1}{\frac{1}{15}+\frac{1}{15}} = \frac{15}{2}$$

$$\left(\frac{\omega}{L}\right)_{BCDE} = \left(\frac{\omega}{L}\right)_{BC} + \left(\frac{\omega}{L}\right)_{DE} = 30+\frac{15}{2} = \frac{75}{2}$$

$$\left(\frac{\omega}{L}\right)_{Peq.} = \frac{1}{\frac{1}{\left(\frac{\omega}{L}\right)_A} + \frac{1}{\left(\frac{\omega}{2}\right)_F} + \frac{1}{\left(\frac{\omega}{L}\right)_{BCDE}}} = \frac{1}{\frac{1}{15}+\frac{1}{15}+\frac{1}{\frac{75}{2}}}$$

$$\left(\frac{\omega}{L}\right)_{Peq.} = \frac{25}{4} = 6.25.$$

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Vidyavardhini's College of Engineering & Technology

Department of Electronics and Telecommunication Engineering

Academic Year 2024-25

Class:	TE	Semester:	V
Course Code:		Course Name:	DVISI

Name of Student:	Chinmay Umesh Upadhye
Roll No.:	48
Assignment No.:	03
Title of Assignment:	
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Legibility	4	4
Demonstrated Knowledge	4	4
Timely submission	2	2
Total	10	10

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Legibility	4	2-3	1-2
Demonstrated Knowledge	4	2-3	1-2
Timely submission	2	1	1

Checked by

Name of Faculty:

Signature:

Date:

12/10/24

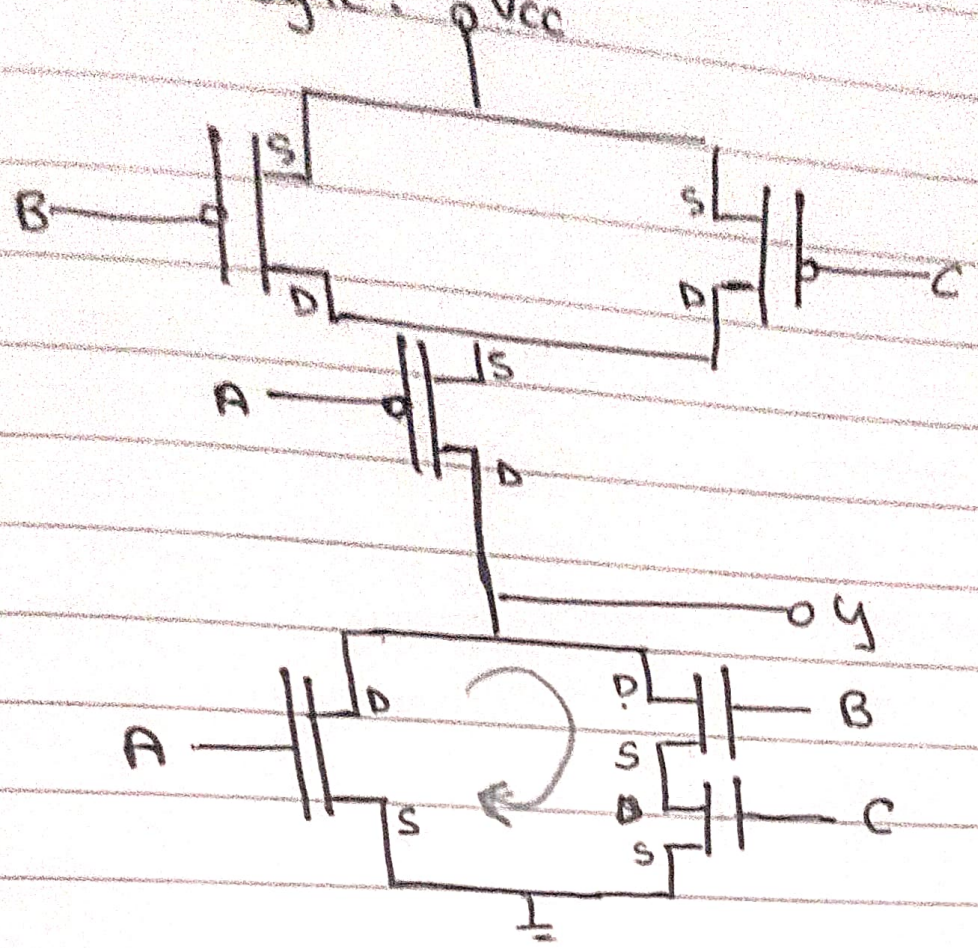
Name: chinmayi Umesh Upadhya
Rollno: 48

Assignment 3

Q1] Realize the following expression using CMOS logic & also draw the layout.

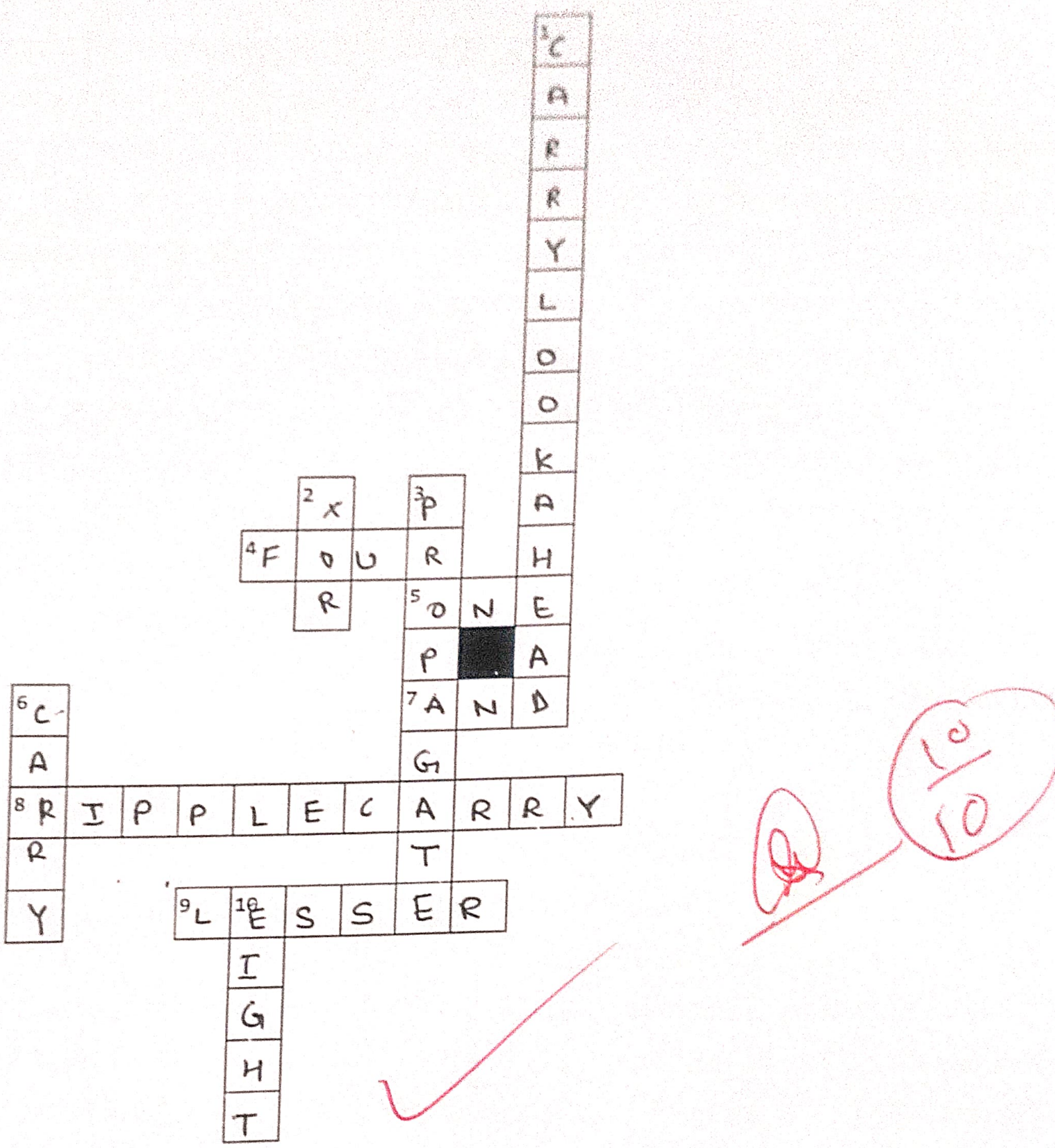
$y = \overline{A + BC}$

Using CMOS logic.



layout :-

Corssword Puzzle on Datapath component - Adder



10/10

Across

4. 4 bit carry lookahead adder uses total delay of _____ gate delay.
5. one full adder is used to add _____ bit
7. In full adder implementation of the carry circuit involves
8. carry propagates in _____ adder

Down

1. more area in _____ adder
2. In full adders the sum circuit is implemented using
3. carry skip adder uses _____ term to skip carry
6. select adder which is uses mux to select carry

9. delay of Hierarchal carry lookahead adder is --- ------ then ripple carry adder

10. for one full adder if 2gate delay then be total gate delay if used in 4 bit ripple c manner